TANDY®

Service Manual

26-3860

Tandy 200

PORTABLE COMPUTER

Catalog Number: 26-3860



CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

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I. INTRODUCTION

This manual is prepared for the Tandy 200 technicians working in the field or in repair centers. Users of this manual should be acquainted with the 80C85A microprocessor, the 81C55 PIO and 82C51A USART. If you are not familiar with these LSIs or need more detailed information, refer to Appendix C in this Service Manual.

This manual is divided into seven sections and three appendices:

Section I
This section provides general information on the Tandy 200 such as specifications, external views and internal views.

Section II
This section describes the disassembly and reassembly procedures.

Section III
This section describes the preventive maintenance and adjustment of the Tandy 200.

Section IV
This section describes the general theory of operation for the Tandy 200.

Section V
This section describes how to troubleshoot the Tandy 200.

Section VI
This section provides a parts list and an exploded view of the Tandy 200.

Section VII
This section provides the schematics, PCB diagrams, and silkscreen views of the PCBs of the Tandy 200.

Appendix A
This appendix provides instructions for installing the optional ROM, additional RAMs and modification jumper module for using the Nickel – Cadmium batteries.

Appendix B
This appendix provides the character code table, keyboard layouts and connector pin assignments.

Appendix C
This appendix provides the technical information of the 80C85A, 81C55, 82C51A and LCD.

System Overview

Tandy 200 portable computer is an enhanced version of the Radio Shack TRS-80 Model 100 Portable Computer. The Tandy 200 is a software compatible with the Model 100 in BASIC so that both system users can take advantage of the large number of programs available.

One important difference between the Model 100 and Tandy 200 is the size of the LCD screen. The Tandy 200's LCD screen is double the size of the Model 100's. That is, the Model 100's display capability is 40 × 8 characters while the Tandy 200 has a display capability of 40 × 16 characters.

The Tandy 200 has the following applications programs in the standard ROMs: BASIC, TEXT, ADDRSS, SCHEDL, TELCOM, MSPLAN, and ALARM.

External View

1 **Keyboard.** Can be used like the standard typewriter. However, the Tandy 200 does have a few special keys. (See Appendix B of this manual for more details.)

2 **LCD Unit.** The Tandy 200 display has sixteen lines that allow 40 characters on each line.

3 **POWER Switch.** Push this switch to turn the power ON or OFF. To conserve the batteries, the Tandy 200 automatically turns the power off if you do not use it for 10 minutes.

4 **Low Battery Indicator.** Before the Tandy 200's operational batteries become exhausted, this indicator will illuminate.

5 **Display Adjustment Dial.** This control adjusts the contrast of the LCD display relative to the viewing angle.

6 **External Power Adapter Connector.** Connect the appropriate end of Radio Shack's AC Power Supply (*Catalog Number 26-3804*, optional/extra) to this connector. Connect the other end of the power supply to a standard AC wall-outlet or approved power strip.

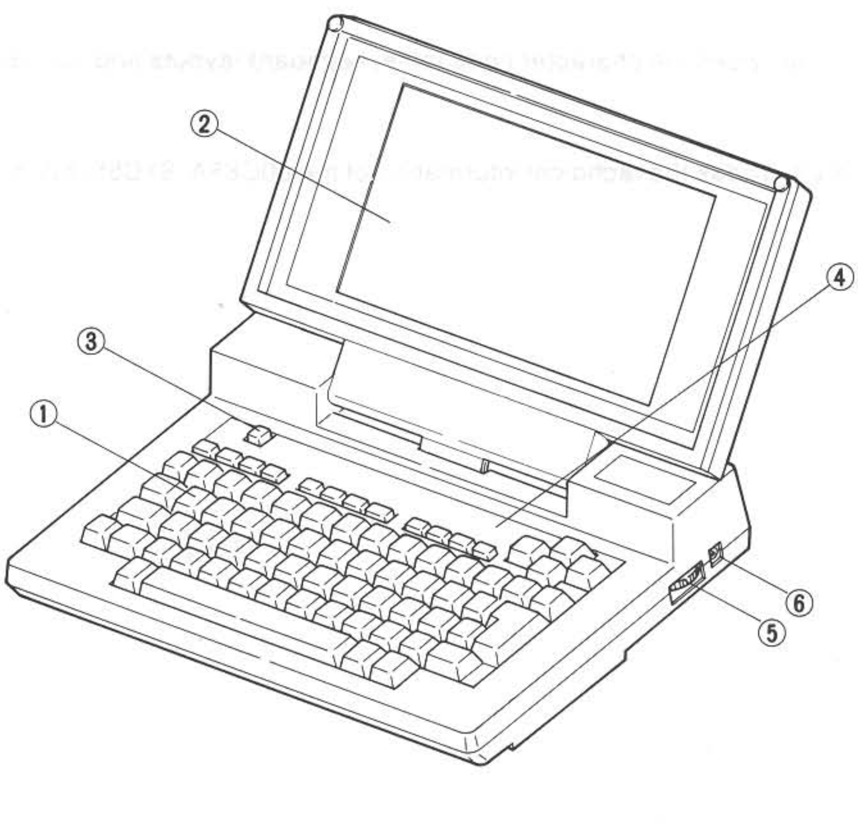


Figure 1-1. Front View

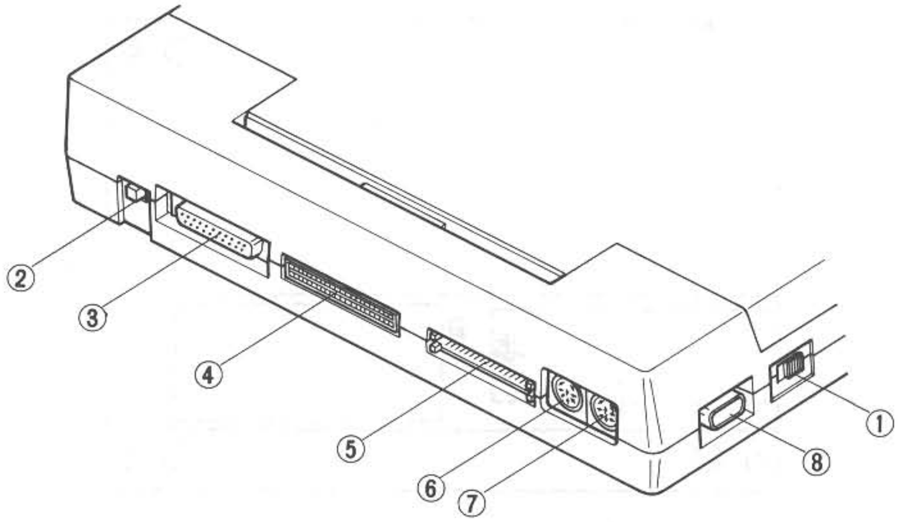


Figure 1-2. Rear View

1 **DIR/ACP Selector.** This selector allows you to select either a direct or acoustic coupler connection. If you are communicating with another computer over the phone lines via the built-in, direct-connect modem, set this switch to the DIR position. If you are using the optional/extra Model 100 Acoustic Coupler (*26-3805*), set this selector to the ACP position.

2 **RESET Switch.** If the Tandy 200 "locks up" (i.e., the display "freezes" and all keys seem to be inoperative), press this button to return to the Main Menu (start-up). It is not likely that the Tandy 200 will lock-up when you are using the built-in applications programs, however, it may occur with customized programs.

3 **RS-232C Connector.** Attach a DB-25 cable (such as Radio Shack *Catalog Number 26-1408*) to this connector when you need to receive or transmit serial information. When communicating directly with another TRS-80 computer, a Null MODEM Adapter (*26-1496*) is required. An 8" Cable Extender (*26-1497*) may also be required.

4 **SYSTEM BUS Connector.** Connect this connector to the TRS-80 Disk/Video Interface (*26-3806*), using the system bus cable.

5 **PRINTER Connector.** For hard-copy printouts of information, attach any Radio Shack parallel printer to this connector, using an optional/extra printer cable.

6 **Direct-Connect MODEM (PHONE) Connector.** When communicating with another computer via the Tandy 200's built-in MODEM, connect the round end of the optional/extra modem cable to this connector.

7 **CASSETTE Recorder Connector.** To save or load information on a cassette tape, connect the cassette recorder here. An optional/extra cassette recorder (and cable) is required.

8 **Bar Code Wand Connector.** Attach the optional/extra bar code wand to this connector. Note that special bar code reader software is required.

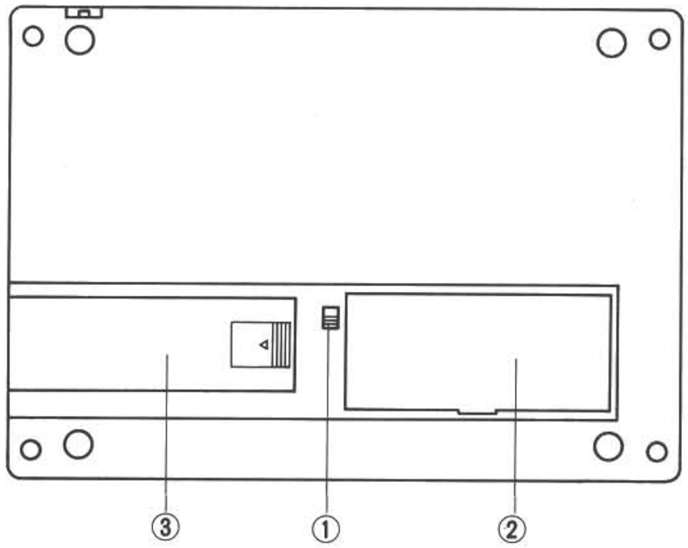


Figure 1-3. Bottom View

1 **MEMORY POWER Switch.** This switch is used to prevent discharge of the internal Nickel-Cadmium battery, which is used for RAM back-up. The Tandy 200 will operate only when the power switch is set to ON. Set this switch to the OFF position when the Tandy 200 will not be used for a long period of time. Note that the RAM will not be backed up when this switch is set to the OFF position.

2 **Optional ROM and RAM Compartment.** An optional/extra ROM and RAMs can be inserted into this compartment to enhance Tandy 200 capabilities.

3 **Battery compartment.** When not connected to an AC power source, the Tandy 200 gets its power from four AA size batteries that must be installed in this compartment.
If the Tandy 200 has the modification jumper module installed Bar Nickel-Cadmium batteries, the battery cover is fixed by a tapping screw and covered by a black sticker.

Internal View

The Tandy 200 consists of four printed circuit boards:

- **LCD PCB**
- **Keyboard PCB**
- **Main PCB**
- **Memory PCB**

[Main electrical components will be shown in these figures.]

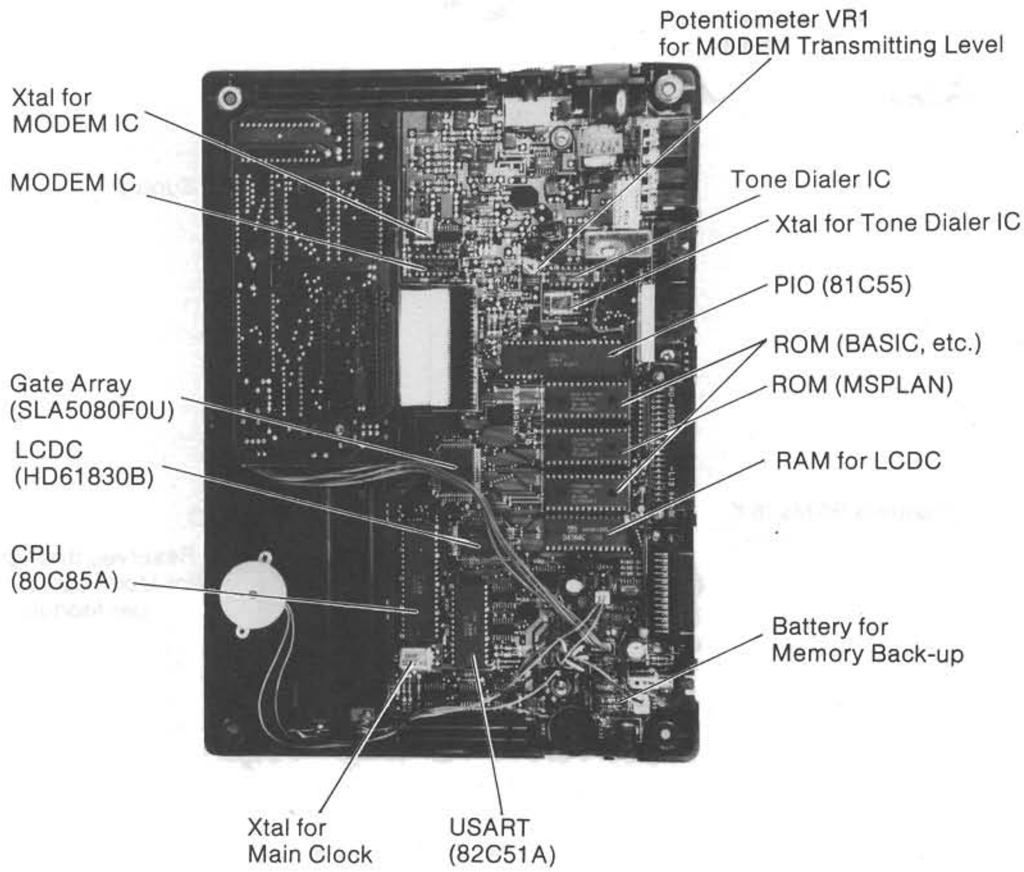


Figure 1-4. Main PCB

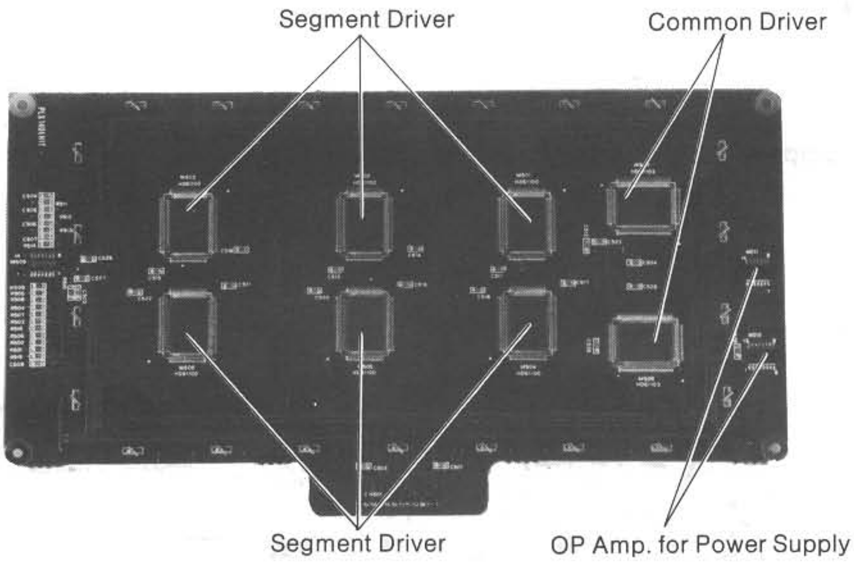


Figure 1-5 LCD PCB

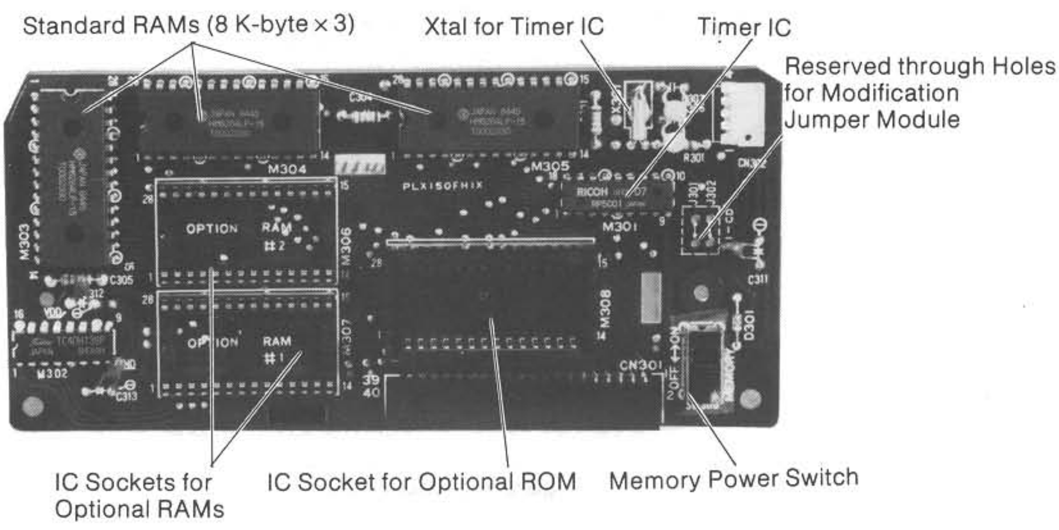


Figure 1-6. Memory PCB

Specifications

Main Components

Keyboard

71 keys (9 x 8 matrix)	
Alphabet keys	27
Number keys	10
Picture-control keys	7
Function keys	8
Special symbol keys	8
Mode keys	5
Other special-use keys	6
LCD display	
Dot pitch	240 x 128 full-dot matrix 1/64 duty 1/9 bias
Dot pitch	0.8 x 0.8 mm
Dot size	0.73 x 0.73 mm
Effective display area	191.2 (W) x 101.6 (D) mm
Operation batteries	
Batteries	Four type AA Alkaline-manganese batteries
Operation time	7 days (at two hours/day) (Note: Without I/O units at normal temperature)
Memory protection battery (on Main PCB)	
Battery	Rechargeable battery
Back-up time	About 15 days (24 KB) About 5 days (72 KB)
Recharge method	Trickle charge by AC adapter or operation batteries
LSIs	
CPU	80C85A Code and pin compatible with 8085
ROM	Maximum 104 KB Standard 72 KB Option 32 KB
RAM	Maximum 72 KB Standard 24 KB RAM Incremental 24 KB RAM on the memory PCB
Dimensions	11-4/5"(L) x 8-4/9"(D) x 2"(H)
Weight	4 lbs. 4 oz.

I/O Interface

RS-232C

Conforms to EIA Standard Signal	TXR (Transmit Data) RXR (Receive Data) RTS (Request to Send) CTS (Clear to Send) DSR (Data Set Ready) DTR (Data Terminal Ready)
Communications Protocol	
Word length	6, 7 or 8 bits
Parity	NON, EVEN, ODD or IGNORE
Stop Bit length	1 or 2 bits
Baud rate	75, 110, 300, 600, 1200, 2400, 4800, 9600, 19200 BPS
Maximum transmission distance	5 meters
Drive maximum voltage output	±5 volts
Drive minimum voltage output	±3.5 volts
Receive maximum voltage input	±18 volts
Receive minimum voltage input	±3 volts

MODEM/Coupler

Conforms to BEL103 Standards	
Data length	6, 7 or 8bits
Parity	NON, EVEN, ODD or IGNORE
Stop bit	1 or 2 bits
Full duplex	Answer mode/originate mode, switchable by software
Other functions	Hang-up function Auto-dialer function

Audio cassette interface

Data Rate	1500 BPS (MARK: 2400 Hz, SPACE: 1200 Hz)

Printer interface

Conforms to Centronics interface standards	
Handshake Signal	$\overline{\text{STROBE}}$, BUSY, $\overline{\text{BUSY}}$

II. DISASSEMBLY INSTRUCTIONS

LCD Case Unit

1. Fully open the LCD case unit until it is locked.
2. Apply force to the upper center portion on the cable cover and remove it by sliding it toward you. Be careful not to damage the cover since this sliding travel is very short.
3. Disconnect the LCD cable from the LCD PCB by pulling it forward.
4. Remove the four screws (a) securing the left and right shaft stoppers and then remove these stoppers. Be careful not to drop the LCD case with its face down.
5. Lift the LCD case unit away from the top cover by moving it in the direction indicated in the Figure 2-1.

Caution:

Do not use longer screws than original ones in the outside screw holes, when re-assembling. It may cause the damage to the LCD bottom case.

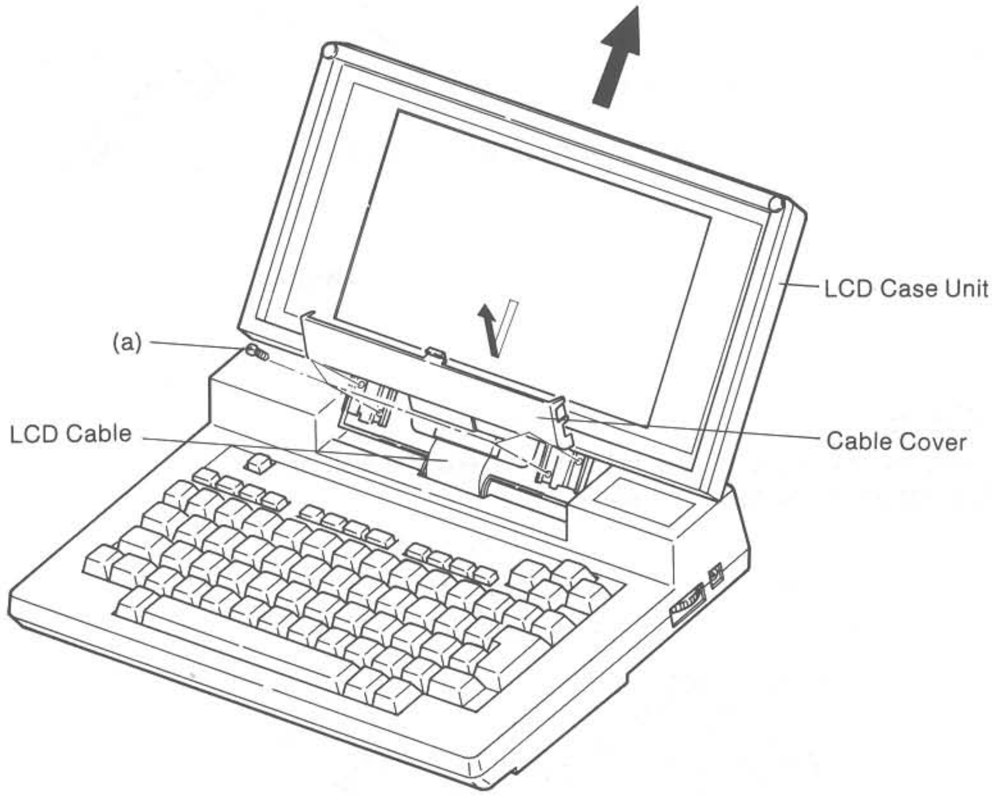


Figure 2-1. LCD Case Removal

LCD PCB

1. Remove the bottom case of the LCD case unit by sliding it toward you. Be careful not to break the snaps off.
2. The LCD PCB is assembled on the bottom case just removed according to the paragraph above. Reposition the bottom case so that the PCB faces up, remove four screws (b) and then lift the PCB away from the bottom case.

To prevent the LCD screen from scratching, we recommend that this removal procedure is performed on a bench covered with a rubber sheet, etc.

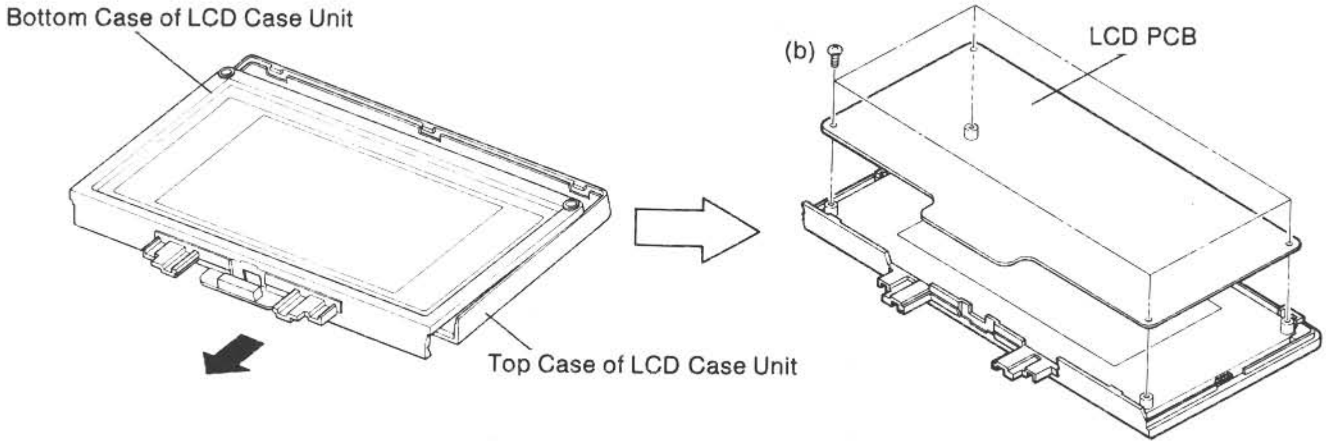


Figure 2-2. LCD PCB Removal

Top Case

1. Remove four screws (c) from the bottom case of the computer.
2. Lift the top case away from the unit.

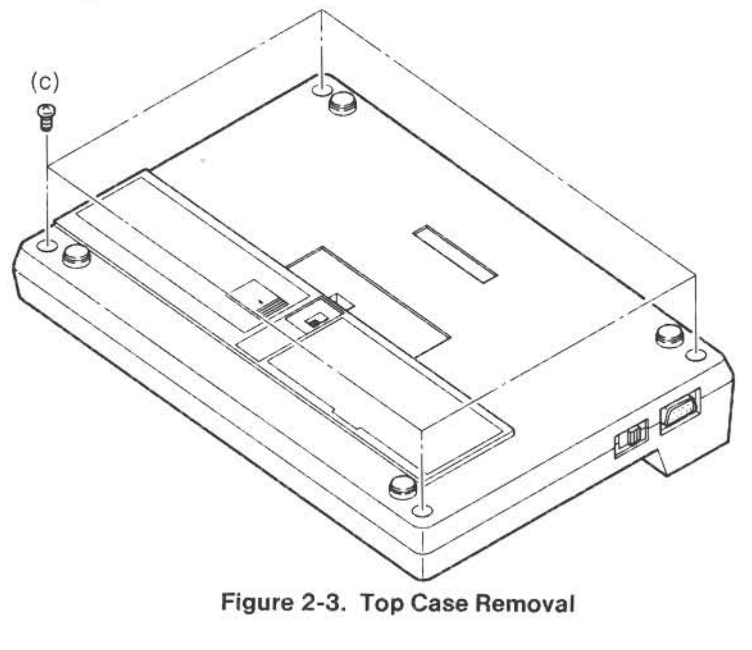


Figure 2-3. Top Case Removal

Keyboard PCB

1. Disconnect the keyboard cable from the main PCB.
2. Remove the keyboard PCB by lifting it away from the bottom case since it is not secured with any screws.

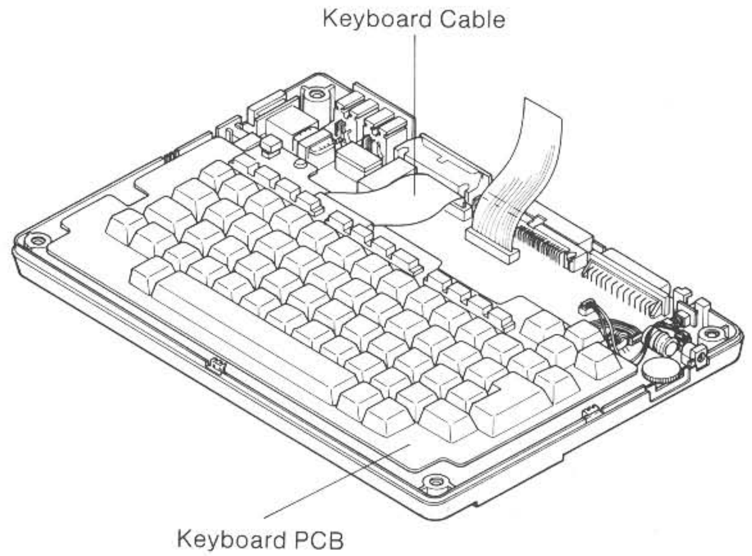


Figure 2-4. Keyboard PCB Removal

Memory PCB

1. This removal should be done after the keyboard PCB removal.
   Remove the 40-pin connector marked CN13 from the Main PCB. Then remove the 4-pin connector marked CN14 from the Main PCB.
2. Remove the screw (d). Unhook the tabs (A, B, C) securing this PCB and remove the memory PCB.

Main PCB

1. Disconnect the 2-pin cables CN9 and CN10 from the Main PCB.
2. Lift the PCB away from the bottom case. Be careful not to lose the knob for the MODEM switch since it is simply inserted into the slider of the switch.

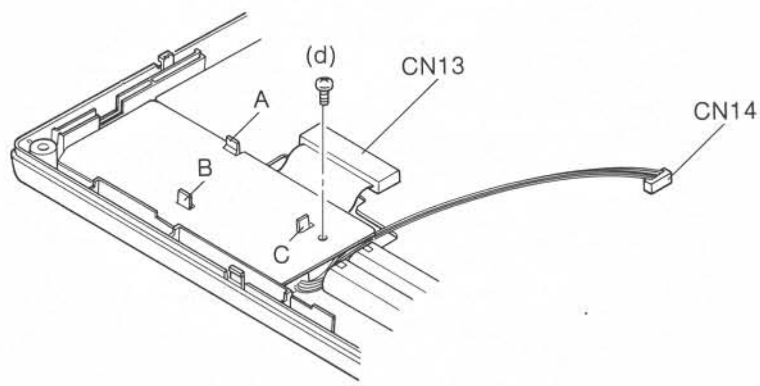


Figure 2-5. Memory and Main PCB Removal

III. PREVENTIVE MAINTENANCE

To clean the body and LCD display

1. To avoid operational trouble, always keep the Tandy 200 clean.
2. Clean the body and the LCD screen using a soft, dry, lint-free cloth.
3. For tough stains, clean the body or the LCD screen with benzol.

Do not use any solvents other than benzol.

MODEM Transmitting Level Adjustment

1. Connect a 600-ohm dummy load between pin-3 (RXMD) and pin-7 (TXMD) of the MODEM connector (CN3).
2. Connect an AC voltmeter across the above dummy load.
3. Set up the Tandy 200 in BASIC mode and enter the following command to generate the carrier signal:

   OUT 178,192

4. Adjust VR1 so as to read -14 to -17 dBm on the AC voltmeter.
5. Then, enter the command:

   OUT 178,194

6. Adjust VR1 so as to read -14 to -17 dBm on the AC voltmeter.
7. Repeat steps 3 to 6 again.

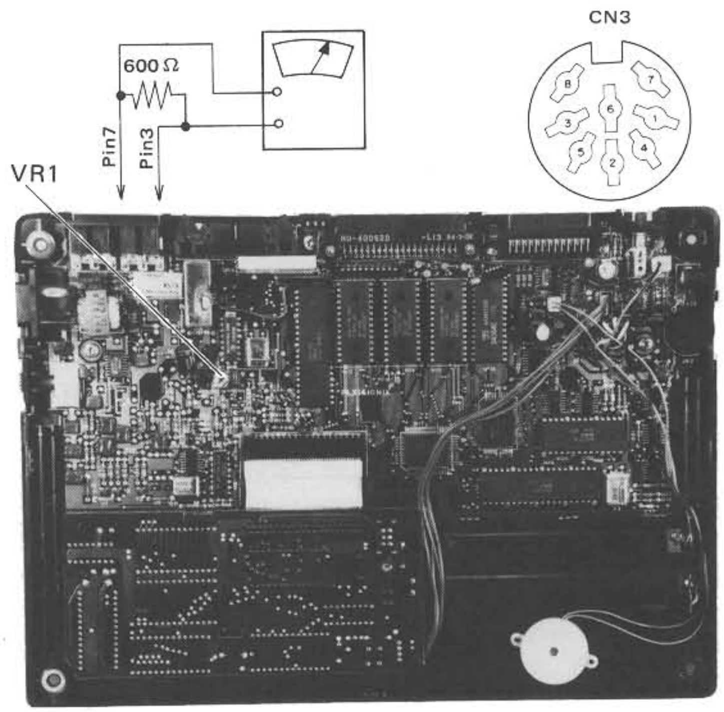


Figure 3-1. MODEM Adjustment

IV. THEORY OF OPERATION

General

This section describes the theory of operation for the Tandy 200. Figure 4-1 shows how this section is organized and highlights significant areas.

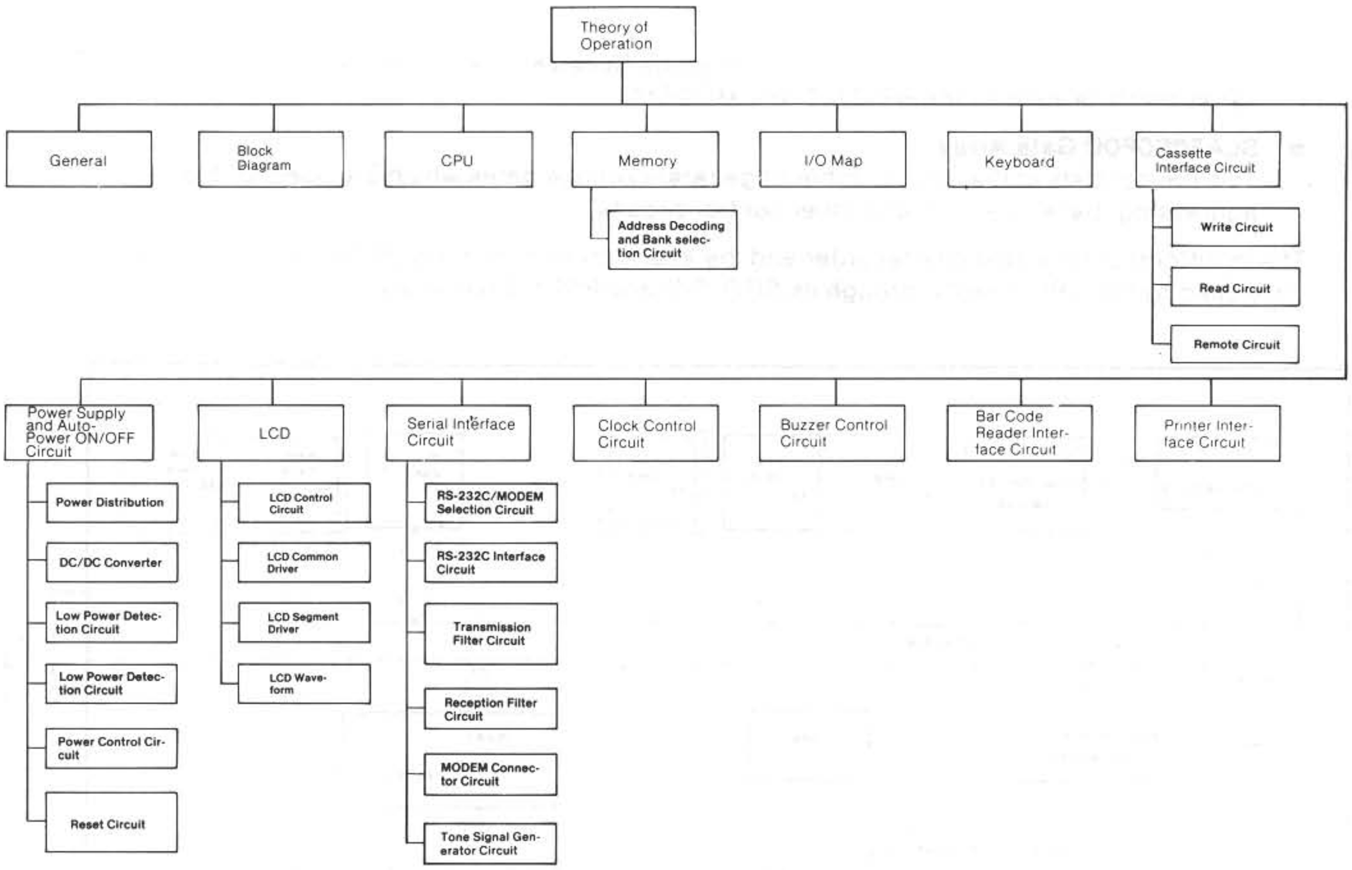


Figure 4-1. Organization of Section IV

Block Diagram

The Tandy 200 has four principal LSIs:

- **80C85A CPU**
  This is the Central Processing Unit which controls all functions.
- **81C55 PIO**
  This is the Parallel Input/Output interface controller which controls the printer interface, keyboard, buzzer, clock, LCD interface and data input of BCR interface.
- **82C51A USART**
  This is the Universal Synchronous/Asynchronous Receiver/Transmitter which controls the serial interface such as the RS-232C and MODEM.
- **SLA5080F0U Gate Array**
  This LSI consists of the large number of general-purpose gates which are used for the I/O addressing, bank selection and other control circuits.

The input/output for a cassette recorder and the interruption from the BCR for the starting data are controlled by the CPU directly through its SOD, SID and RST 5.5 terminals.

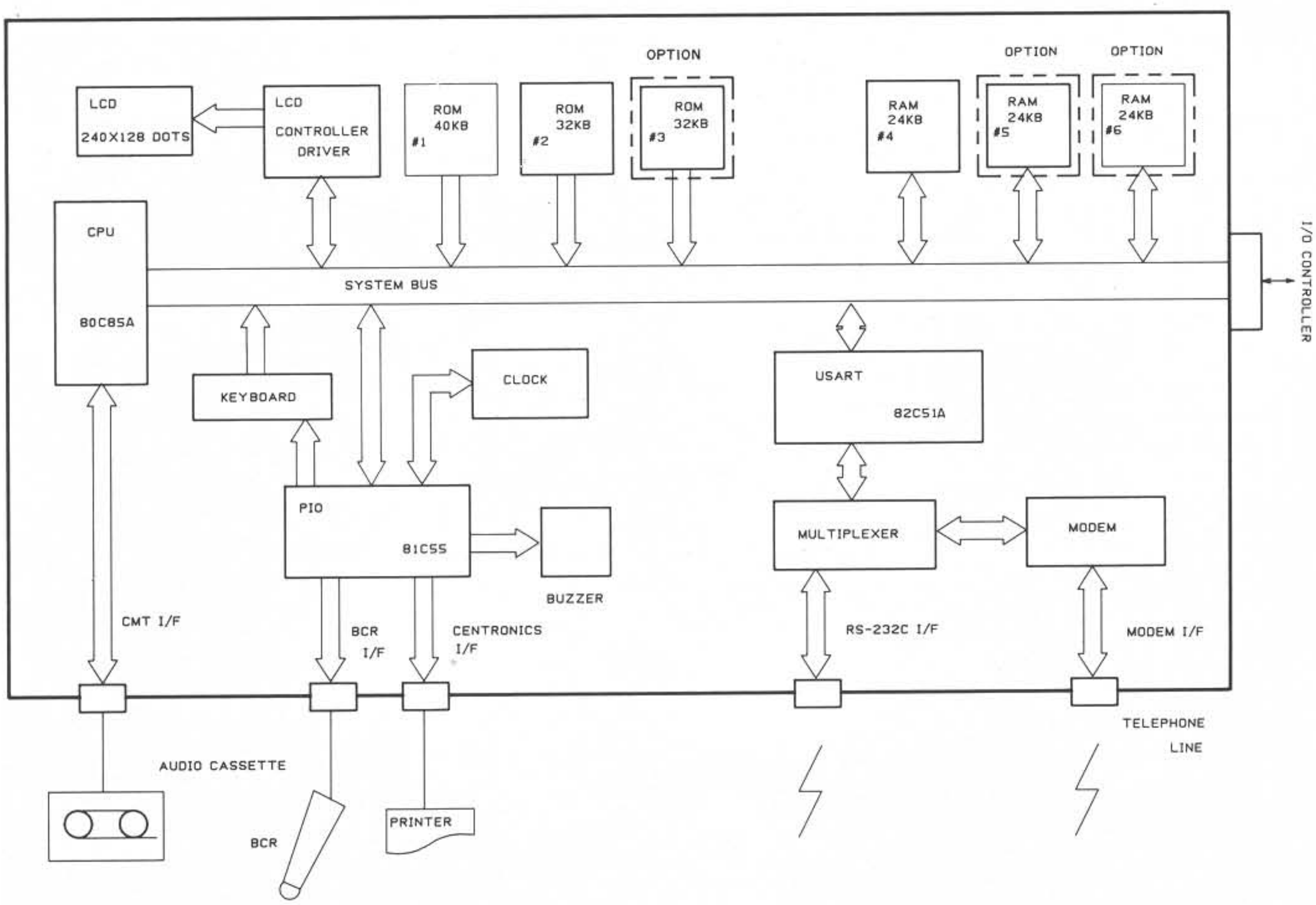


Figure 4-2. Block Diagram

CPU

The CPU is an 80C85A that runs at a clock speed of 2.4576 MHz. It is an 8-bit, parallel Central Processing Unit using C-MOS technology. The instruction set is fully compatible with the 8085A microprocessor. The 80C85A uses a multiplexed data bus. The CPU bus is divided into two sections — the 8-bit address bus named the A8-A15, and the 8-bit address and data bus named the AD0-AD7. The address and data bus are separated in the SLA5080F0U by using the ALE signal. The functional block diagram of this circuit in the SLA5080F0U is shown in Figure 4-3.

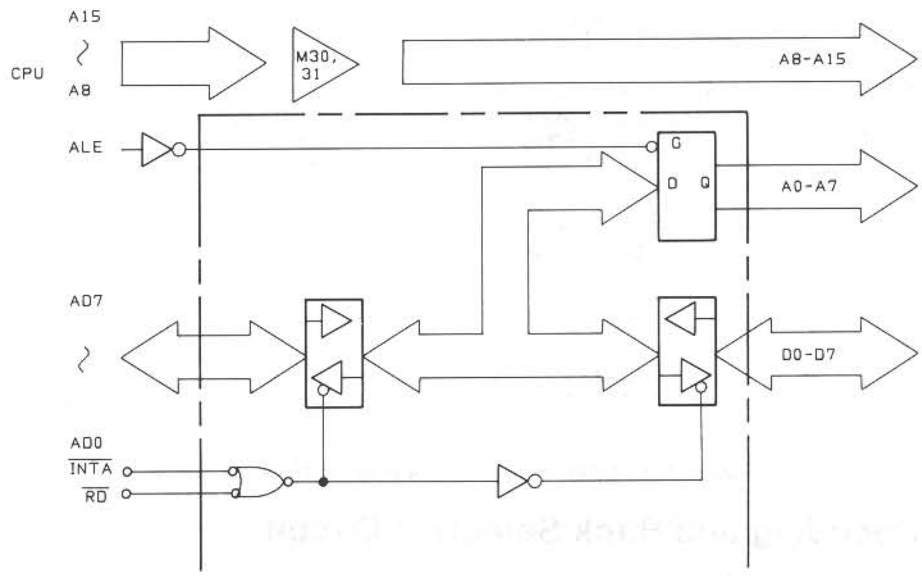


Figure 4-3. Functional Block Diagram of Bus Separation Circuit

Memory

The Tandy 200 uses a 32K-byte ROM for the MSPLAN, 40K-byte ROM for BASIC and the other application programs, and 24K-byte static RAM to store the data and programs. The 40K-byte ROM consists of an 8K-byte ROM (M13) and 32K-byte ROM (M15). The 24K-byte RAM consists of three 8K-byte RAMs.

Furthermore, a 32K-byte ROM and two 24K-byte RAM packages can be used optionally. The 24K-byte RAM package consists of three 8K-byte RAMs and one decoder IC (40H138), mounted on a ceramic substrate.

Figure 4-4 shows the memory map and Figure 4-5 shows the internal wiring diagram of the RAM package.

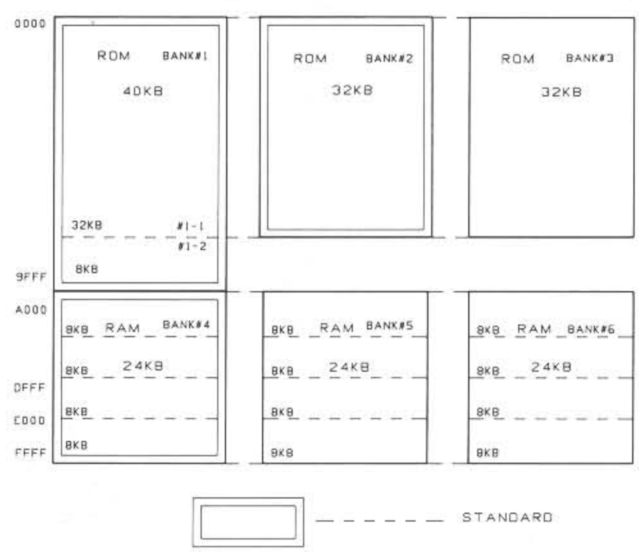


Figure 4-4. Memory Map

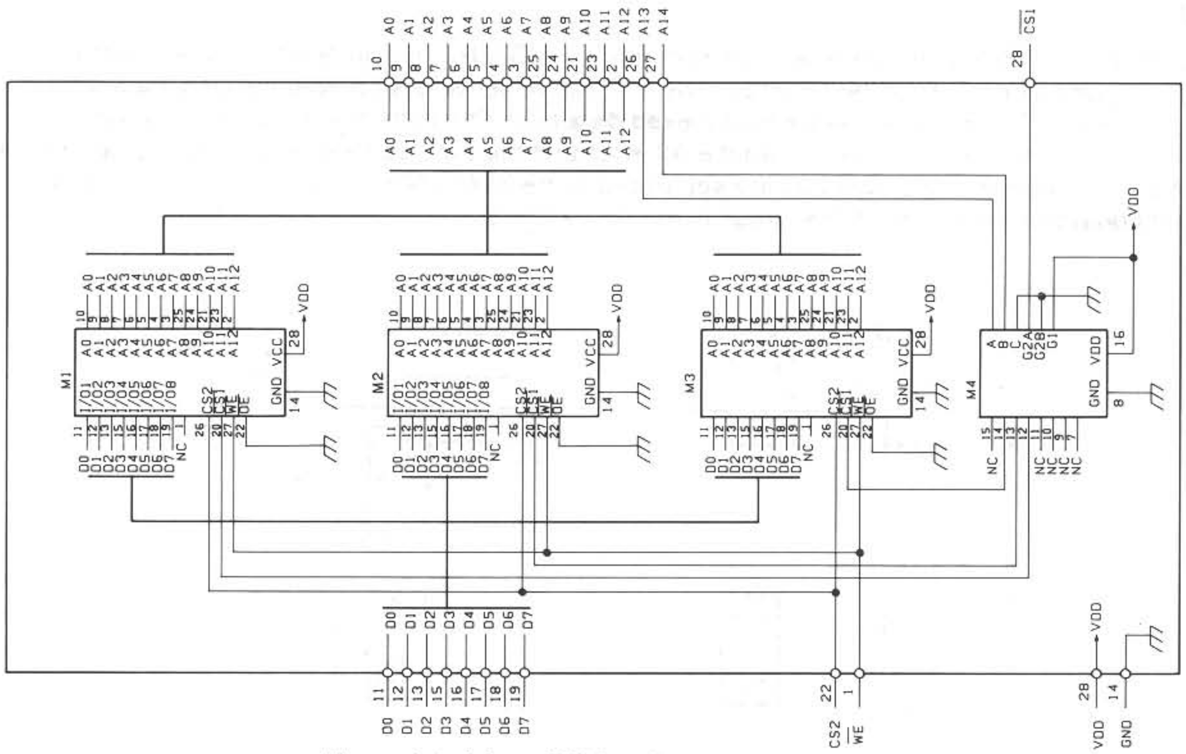


Figure 4-5. Internal Wiring diagram of RAM package

Address Decoding and Bank Selection Circuit

Selection of RAMs and ROMs are determined by the address and bank signals generated in the SLA5080F0U.
Figure 4-6 shows the bank selection circuit in the SLA5080F0U.
The latch AA0036 stores the bank selection data sent from the CPU with the $\overline{Y5}$ and $\overline{WR}$ signal. The decoder AA0038 is enabled by the memory address 0000H to 9FFFH for ROMs and the decoder AA0037 is enabled by the memory address A000H to FFFFH for RAMs.

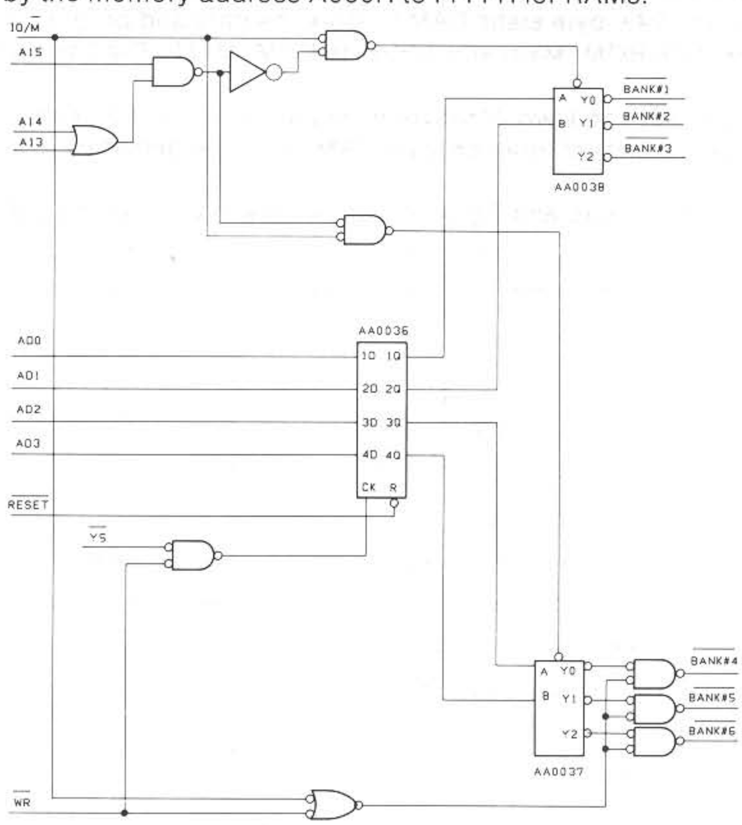


Figure 4-6. Bank Selection Circuit

I/O Map

Figure 4-7 shows the I/O address decoding circuit included in the SLA5080F0U that decodes address signals AD4-AD6. The AD7 signal acts as the enable signal for the decoder AA0024 with the IO/$\overline{M}$ signal. At the latch AA0063, the chip enable terminals $\overline{G1}$ and $\overline{G2}$ are connected to the ALE signal passing through the inverter, because the AD0-AD7 signals are the multiplexed bus. The I/O map and I/O port description are shown in Figure 4-8.
The port assignment of the 81C55 is shown in Table 4-1.

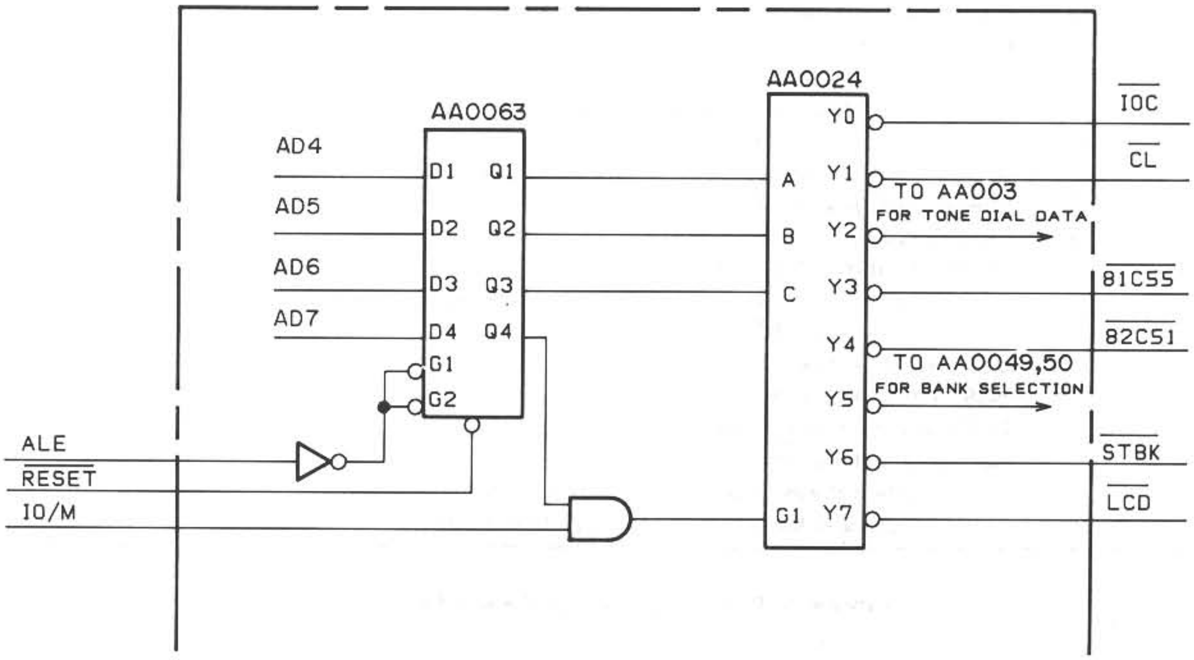


Figure 4-7. I/O Address Decoding Circuit

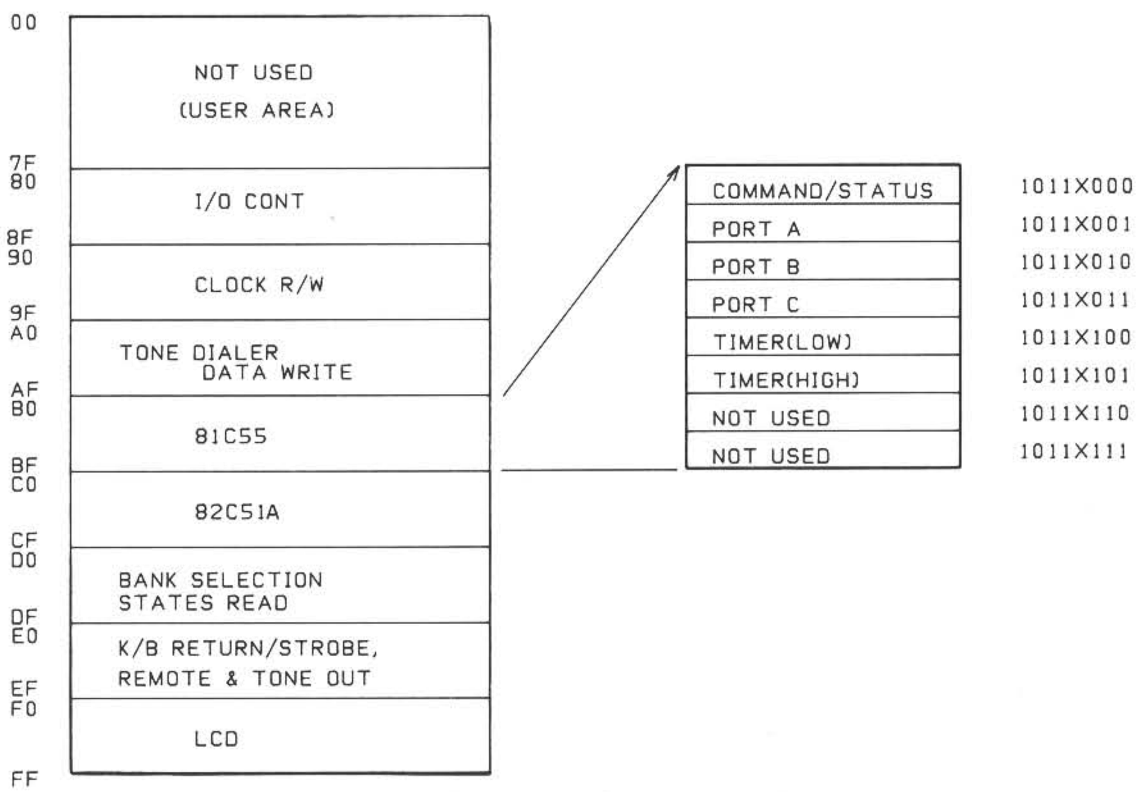


Figure 4-8. I/O Map and I/O Port Description

Port Assignment of 81C55

Terminal	I/O	Description
PA0	O	Print Data 0, Key Scan 0
PA1	O	Print Data 1, Key Scan 1
PA2	O	Print Data 2, Key Scan 2
PA3	O	Print Data 3, Key Scan 3
PA4	O	Print Data 4, Key Scan 4
PA5	O	Print Data 5, Key Scan 5
PA6	O	Print Data 6, Key Scan 6
PA7	O	Print Data 7, Key Scan 7
PB0	O	Print Data 8, Key Scan 8
PB1	O	ORIG/ANS Output ("H" = ORIG, "L" = ANS)
PB2	O	BUZZER Output (Active "L")
PB3	O	$\overline{\text{RS232C}}$ ("H" = Modem select, "L" = RS-232C select)
PB4	O	Power Cut Signal (PCS) Output (Active "H")
PB5	O	BELL Output
PB6	O	Modem Enable (MEN) Output (Active "H")
PB7	O	CALL Output (Active "H") Connects and disconnects the telephone line.
PC0	I	Low Power Sence ($\overline{\text{LPS}}$) Input (Active "L")
PC1	I	$\overline{\text{BUSY}}$ Input (Active "L")
PC2	I	BUSY Input (Active "H")
PC3	I	BCR Data Input (black line = "H", white line = "L")
PC4	I	Carrier Detect (CD) Input
PC5	I	Carrier Detect Break Down (CDBD) Input (Active "H")
TO	O	Clock Output and Melody Output for 82C51A (USART)

Table 4-1. Port Assignment of the 81C55

Keyboard

Key strobe signals are emitted from the PB0 and PA0-PA7 terminals of the 81C55, and the return signals from the keyboard pass through the octal bus buffer (M27) which is enabled by NANDing the $\overline{\text{RD}}$ and $\overline{\text{STB/K}}$ signals at M29, and then the return signals are sent to the CPU.
The $\overline{\text{STB/K}}$ signal is generated in the SLA5080F0U when the CPU assigns E0-EFH to the I/O port address. The CPU starts the key scan operation when the RST 7.5 interruption is accepted. This interruption (TP signal) is generated about every 3.3 msec. at M34 by dividing the CLK signal (2.4576 MHz).
Condition of pressing "T" key is shown in Figure 4-9.

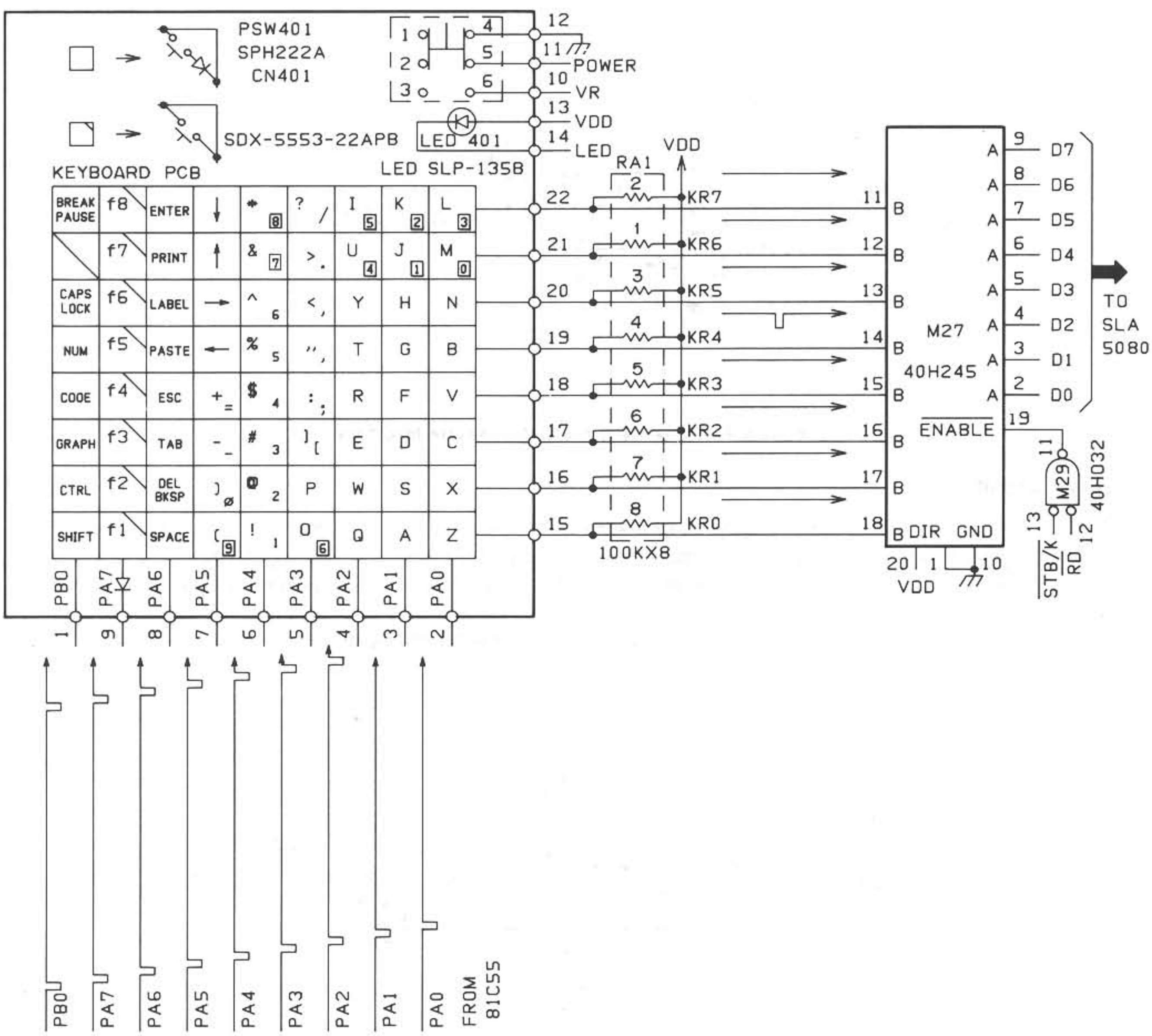


Figure 4-9. Condition of Pressing "T" Key

Cassette Interface Circuit

The cassette interface circuit is subdivided into three sections:

- **Write Circuit**
- **Read Circuit**
- **Remote Circuit**

Write Circuit

The write circuit is accomplished in several steps. First, the serial data from the SOD terminal of the CPU is inverted by M1. Then, the DC component is removed by C3. And finally, the data passes through an integrator consisting of R8 and C2, and after voltage division, out to a cassette recorder AUX jack.
Figure 4-10 shows the write circuit of the cassette interface.

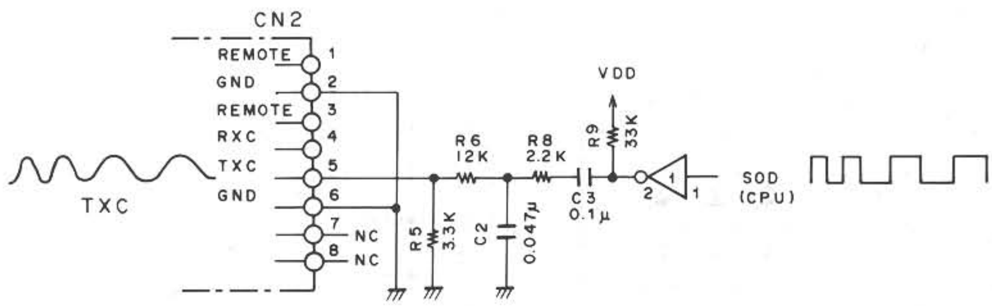


Figure 4-10. Write Circuit of Cassette Interface

Read Circuit

The signal input from the earphone jack of the cassette recorder passes through the clamp circuit consisting of D1 and D2, and then is input to the comparator circuit consisting of M2.
Finally, the signal is converted into the digital signal and sent to the SID terminal of the CPU. Figure 4-11 shows the read circuit.
In this circuit, D8 clamps the negative voltage output of the comparator.

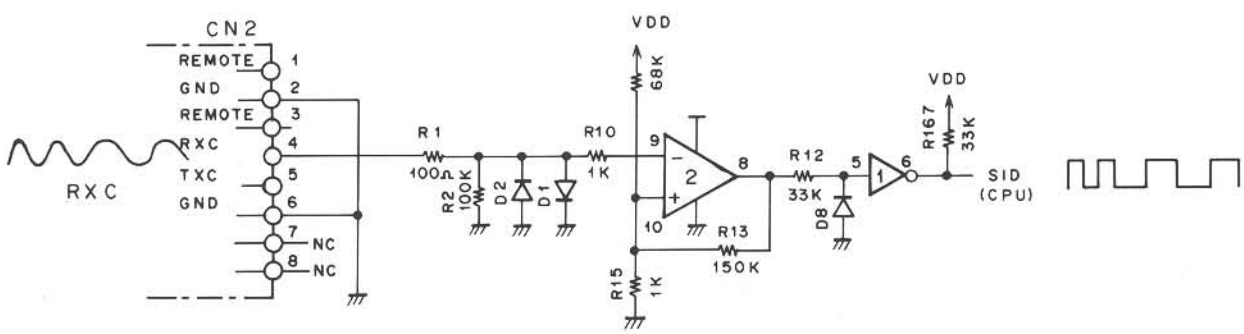


Figure 4-11. Read Circuit of Cassette Interface

Remote Circuit

By writing-in data "1" into bit 1 of the output port specified by E0-EFH, the REMOTE terminal of the SLA5080F0U is changed to "H." Then T11 is switched ON and RY1 is energized. This controls the motor of the cassette recorder.

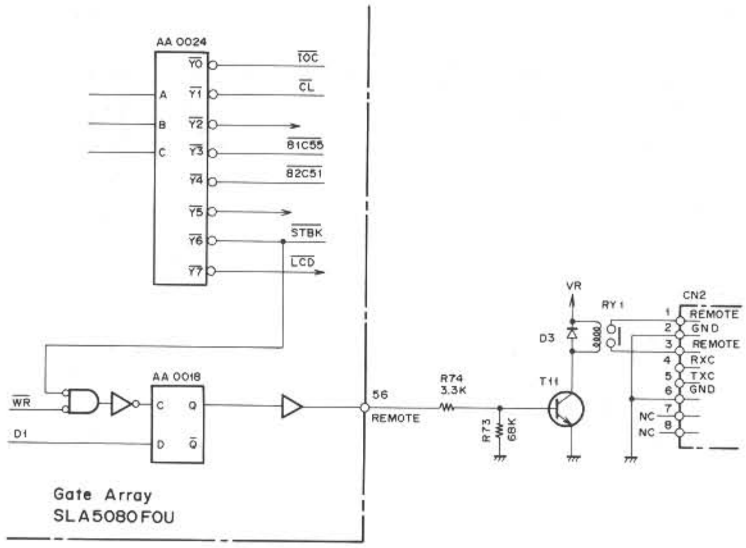


Figure 4-12. Remote Circuit of Cassette Interface

Printer Interface Circuit

The printer interface circuit conforms to Centronics standards. As shown in Figure 4-13, the BUSY signal from the printer is read from the PC2 of the 81C55. If the condition is not busy (PC2="L"), the 8-bit parallel data (PA0-PA7 from 81C55) is sent to the printer. Then, by writing-in data "1" into bit 1 of the output port specified by I/O address E0-EFH, the $\overline{\text{PSTB}}$ signal is generated in the SLA5080F0U and sent to the printer.

As soon as the printer receives this $\overline{\text{PSTB}}$ signal, the BUSY signal is changed to "H" indicating that the printer is busy. The CPU then waits for a while until this BUSY signal becomes "L." As soon as the printer prints the one character specified by the 8-bit parallel data, the BUSY signal becomes "L." Then, the CPU sends the next 8-bit parallel data.

If the printer is in ON LINE condition, the $\overline{\text{BUSY}}$ signal is "H" and sent to the CPU, passing through the PC1 of the 81C55. But, when in the OFF LINE condition, the $\overline{\text{BUSY}}$ signal is "L" and transmission of print data to the printer is inhibited by the CPU.

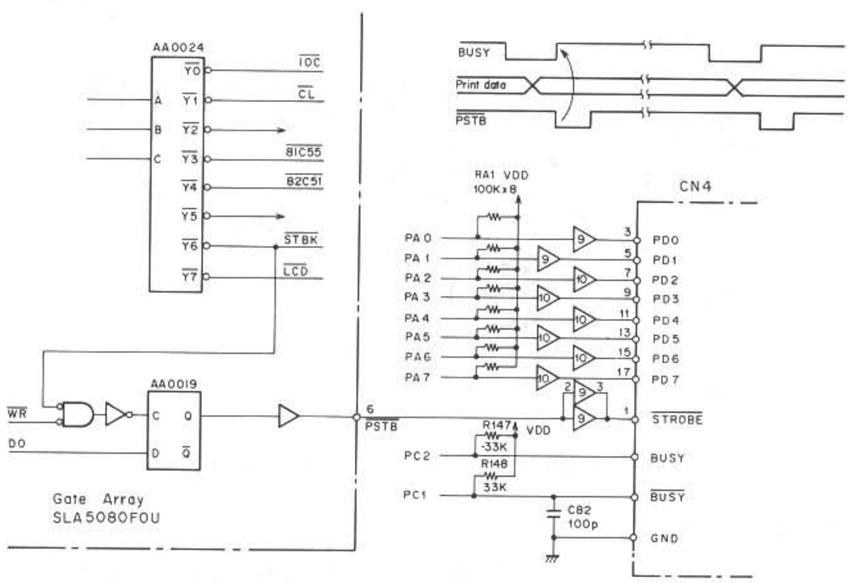


Figure 4-13. Printer Interface Circuit

Bar Code Reader Interface Circuit

The input signal from the bar code reader is subjected to waveform shaping, inverted by the Schmitt-type inverter (M1), and then sent to the PC3 terminal of the 81C55 and the RST 5.5 terminal of the CPU.

When the bar code reader reads the first white part of the bar code, a "L" level signal is generated, then inverted by M1. As soon as RST 5.5 interruption occurs, the CPU starts the data input operation, passing through the PC3 of the 81C55. As the bar code reader is moved across the bars, "H" and "L" signals (which correspond to white and black bars respectively) are generated continuously and inversion signals are sent to the PC3 of the 81C55 as the serial input data. Refer to Figure 4-14.

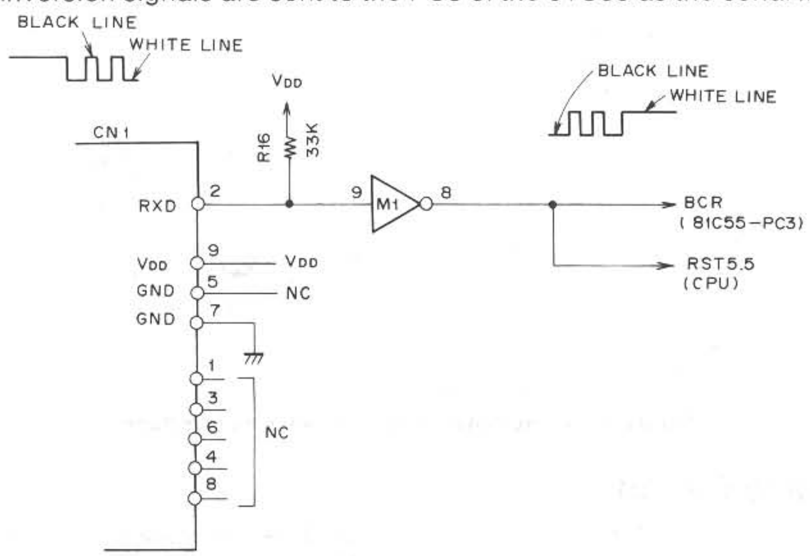


Figure 4-14. Bar Code Reader Interface Circuit

Buzzer Control Circuit

There are two ways to operate the buzzer. One is to sound the buzzer with the specified frequency by emitting a signal from the PB5 terminal of the 81C55 and the other, by using timer output (TO), and the BUZZER signal (PB2) of the 81C55. In addition, the BELL signal also acts as the control signal of the DC/DC converter circuit during the power-up sequence (refer to the Power Control Circuit).

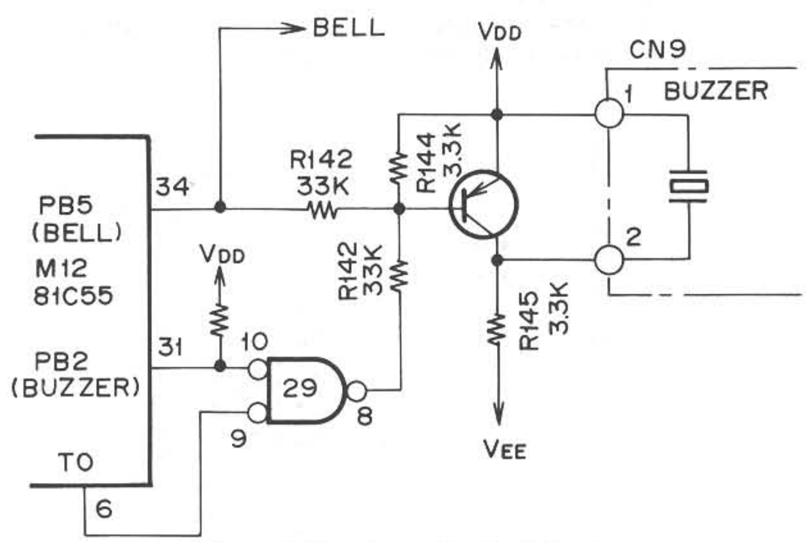


Figure 4-15. Buzzer Control Circuit

Signal from the PB5 of the 81C55

When the PB2 of the 81C55 is "H," the buzzer sounds by repeated switching of the buzzer driving transistor. This is caused by "H", "L", "H", "L" . . . output signals from the PB5 synchronizing with the frequency for sounding the buzzer. This method is used for the BEEP command in BASIC.

Using the 81C55 Timer Output

In this method, the buzzer is made to sound by setting the 81C55 timer in the square wave output mode. To write the value corresponding to the sound frequency, the CPU assigns B4, B5, BC or BD to the I/O port address. This frequency is assigned by the first parameter of the SOUND command in BASIC.
If the above procedures are completed, the TO terminal of 81C55 outputs the square waves, and the PB2 of the 81C55 controls the length of the sound whenever the PB5 is "L." How long the sound is heard depends on the second parameter of SOUND command in BASIC.

Clock Control Circuit

A TIMER IC (RP5C01) on the memory PCB is used in the clock control circuit so that the current time and alarm time can be set and read by the commands in BASIC.
To set and read the time, the CPU assigns 90-9FH to the I/O port address.
In addition, because the back-up power VB is supplied to the TIMER IC, the clock and alarm functions are enabled even when the Tandy 200 is in the power-off condition.
Figure 4-16 shows the internal block diagram, and Table 4-2 shows the I/O port address assignment of each function. An internal 26 × 4-bit RAM is used as a buffer memory when the data is transmitted between RAM banks.

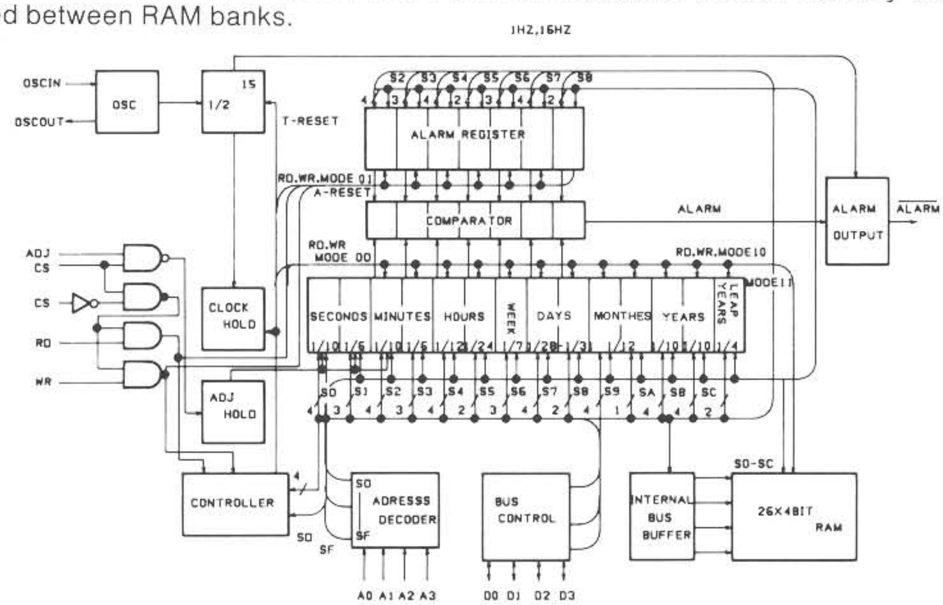


Figure 4-16. RP5C01 Internal Block Diagram

Address Assignment of RP5C01

MODE	MODE 00					MODE 01					10	11
A3 ~ A0	Description	D3	D2	D1	D0	Description	D3	D2	D1	D0	Description	
0	One sec. Counter						×	×	×	×		
1	Ten sec. Counter	×					×	×	×	×		
2	One min. Counter					Alarm One sec. Register					10	11
3	Ten min. Counter	×				Alarm Ten min. Register	×					
4	One hour Counter					Alarm One hour Register						
5	Ten hours Counter	×	×			Alarm Ten hours Register	×	×			4bit	4bit
6	Day Counter	×				Alarm Day Register	×				×	×
7	One day Counter					Alarm One day Register					13	13
8	Ten days Counter	×	×			Alarm Ten days Register	×	×				
9	One month Counter						×	×	×	×	RAM	RAM
A	Ten month Counter	×	×	×		12/24 Hours Selector	×	×	×			
B	One year Counter					Leap Year Counter	×	×				
C	Ten years Counter						×	×	×	×		
D	Mode Register	Timer EN	Alarm EN	M1	M0		Timer EN	Alarm EN	M1	M0	←	←
E F	Test Register Reset Controller etc.	Test 3 1 Hz ON	Test 2 16 Hz ON	Test 1 Timer Reset	Test 0 Alarm Reset		Test 3 1 Hz ON	Test 2 16 Hz ON	Test 1 Timer Reset	Test 0 Alarm Reset	←	←

×: Don't care when writing, always "0" when reading.

Table 4-2. RP5C01 I/O Port Address Assignment

To set and read the time and alarm information, the CPU proceeds in the sequence following.

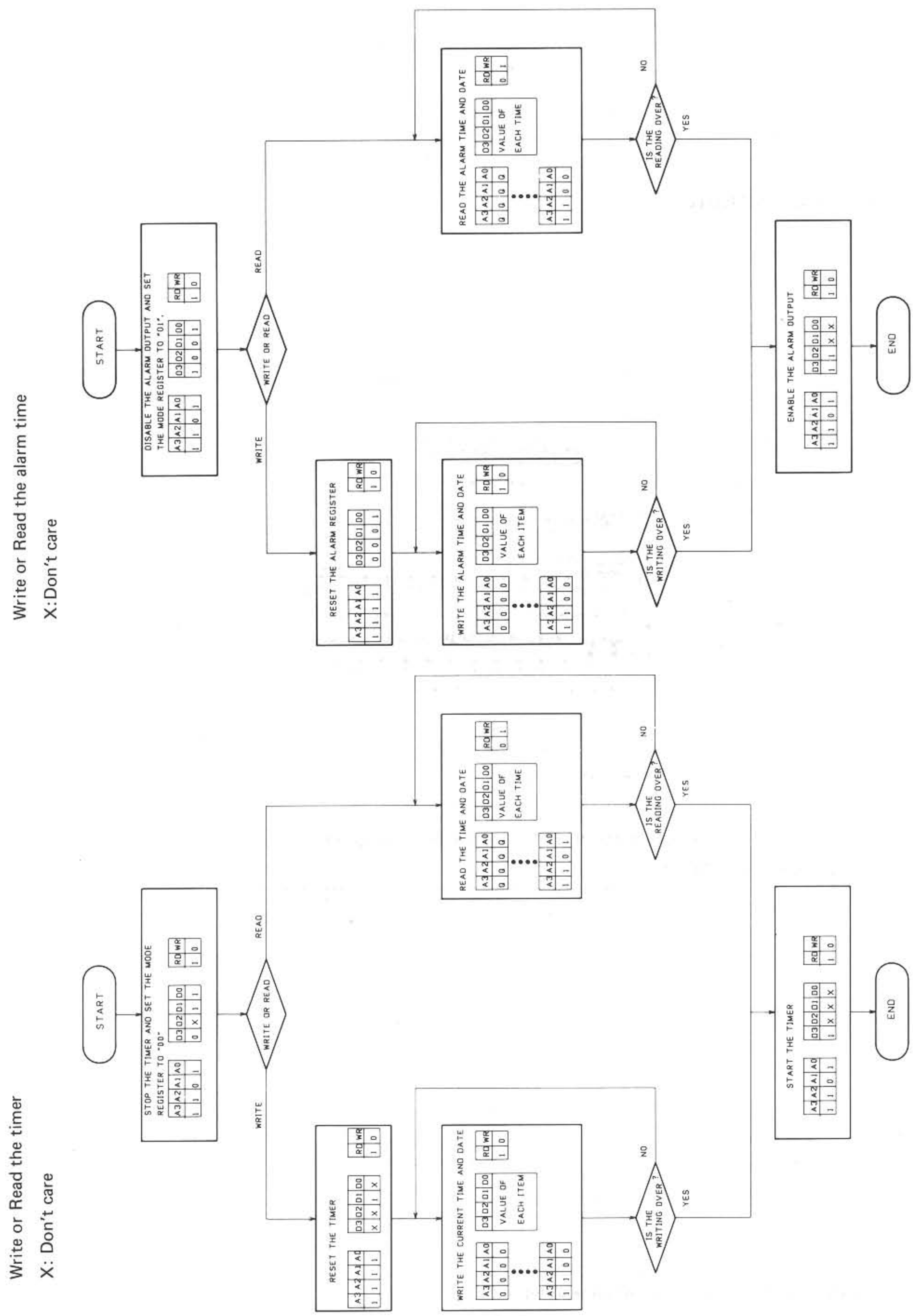


Figure 4-17. Flowchart for the TIMER IC

Serial Interface Circuit

The serial interface circuit supports asynchronous serial transmission/reception.
The heart of this circuit is the 82C51A (USART). It performs the job of converting the parallel byte data from the CPU to a serial data stream including start, stop and parity bits.
For a more detailed description of how this IC performs these functions, refer to Appendix C of this manual.
Figure 4-18 shows the functional block diagram of the serial interface circuit. In this figure, the TO signal, basic timing clock for the USART, defines the transmission/reception baud rate.
To transmit and receive the serial data from external devices, the $\overline{RS232C}$ signal selects either MODEM or RS-232C interface. During the MODEM operation, the ORGIS signal switches either the originate mode or answer mode for the MODEM IC.
The serial interface circuit is subdivided into the following circuits:

- **RS-232C/MODEM Selection Circuit**
- **RS-232C Interface Circuit**
- **MODEM IC**
- **Transmission Filter Circuit**
- **Reception Filter Circuit**
- **MODEM Connector Circuit**
- **Tone Signal Generator Circuit**

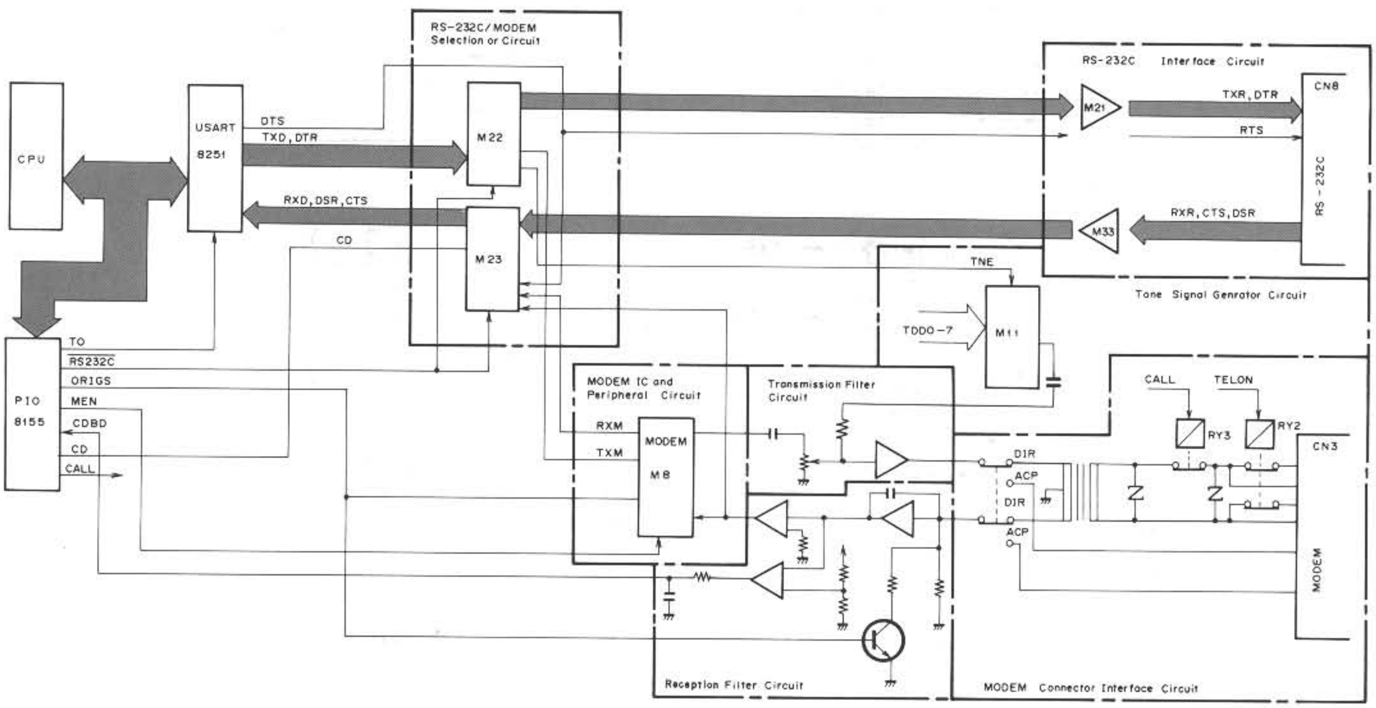


Figure 4-18. Functional Block Diagram of the Serial Interface

RS-232C/MODEM Selection Circuit

The $\overline{RS232C}$ signal (PB3 terminal of the 81C55) determines whether the serial port is to be used as RS-232C or as MODEM. When the $\overline{RS232C}$ signal is "L," the serial port is used as RS-232C. When the $\overline{RS232C}$ signal is "H," the port is used as MODEM.
The reception signal, including the control signal, is demultiplexed at M23. The transmission signal is multiplexed at M22.

During the RS-232C mode, the CD (Carrier Detect) signal is not used. To make this condition, pin 14 of M23 is connected to the ground.

During the MODEM mode, the RTS signal is used as the self-loopback signal and it is sent back to the CTS terminal. The DSR signal is not used in the Tandy 200 USA version, since the TD signal is always fixed to "H" level by the hardware. The CD signal selects the CDD signal from the RXCAR terminal of the MODEM IC. Because the CPU detects the carrier signal by counting the frequency of the CDD signal corresponding with the originate mode or answer mode. When a customer uses the tone dialer function, the DTR signal acts as the enable signal for the tone dialer IC.

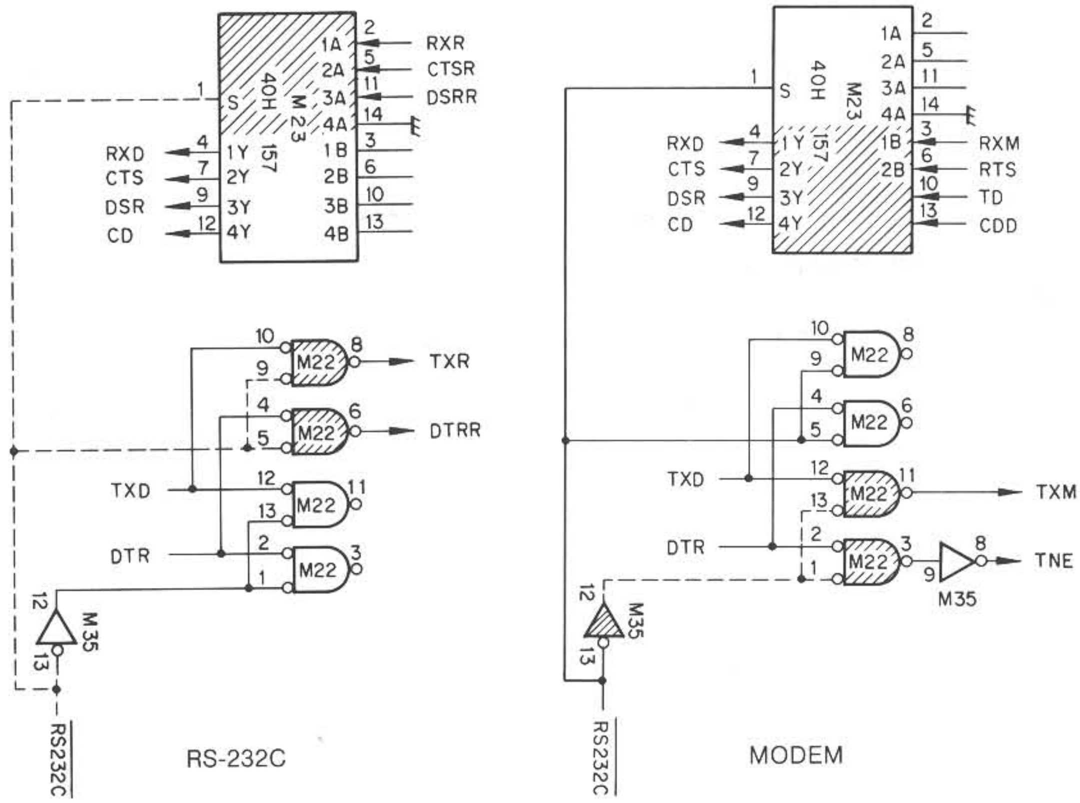


Figure 4-19. RS-232C/MODEM Selection Circuit

RS-232C Interface Circuit

In the RS-232C transmission circuit, after the DC component is removed from the signals by the coupling capacitors, the signals are leveled to ±5V signals by the inverters connected in parallel, and then are output as RS-232C transmission signals. In the RS-232C reception circuit, the DSRR, CTSR, and RXR signals from the external RS-232C line are subjected to waveform shaping and inverted by M33, and then converted to +5V or ground level signals by the diodes. The signals are then demultiplexed at M23 and converted to CTS, DSR and RXD signals which are input to the 82C51A. The CD signal is not used in the Tandy 200.

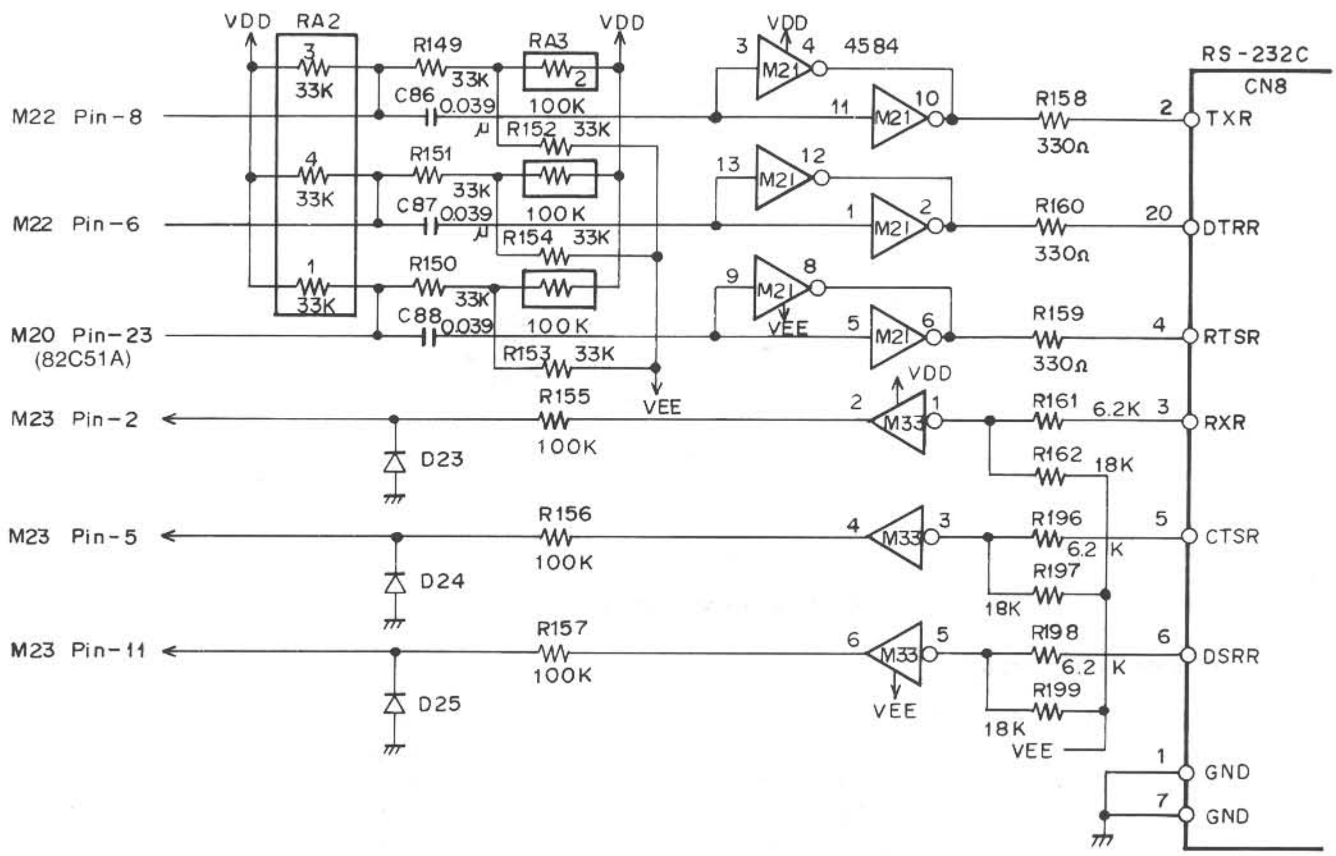


Figure 4-20. RS-232C Interface Circuit

MODEM IC

The Tandy 200 employs the IC MC14412 as a MODEM control device. This IC modulates/demodulates data to be transmitted/received in accordance with frequencies suitable for originate or answer mode respectively.
The RXRATE and TYPE terminals of MC14412 (M8) are pulled up to VDD.
The baud rate is set to 300 bps, and the U.S. Standard is selected. Since the ECHO and SELF TEST terminals are not needed, they are connected to ground.
The PB6 terminal of the 81C55 outputs the enable signal (MEN) for the MODEM IC until the unit is in the MODEM mode.
In addition, the signal designated by the ORIG-ANS parameter in TELCOM mode is input to MODE input terminal, and it switches between the originate mode or the answer mode. This signal is output from the PB1 terminal of the 81C55.

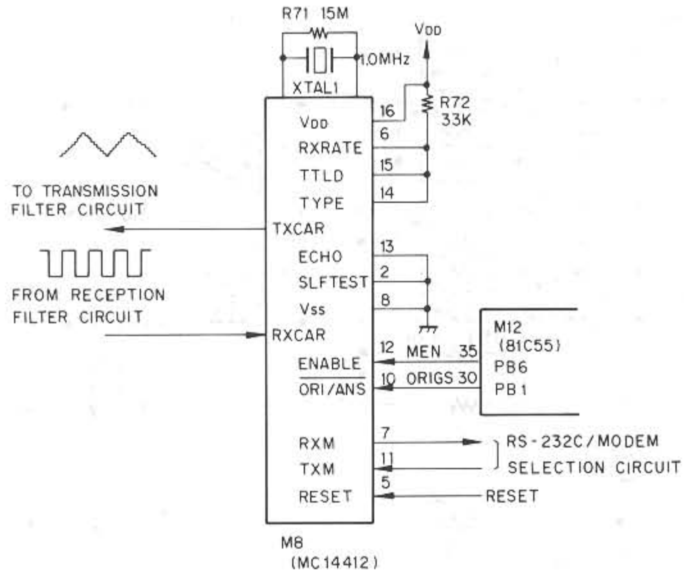


Figure 4-21. MODEM IC and Peripheral Circuit

Transmission Filter Circuit

The DC component of the carrier output from the TXCAR terminal is removed by C50. The signal level is adjusted by the potentiometer VR1. The signal then passes through the transmission band-pass filter and is sent to the telephone line or the acoustic coupler.
The transmission filter circuit is composed of an active filter (consisting of an operation amplifier) and the intermediate frequency of the active filter is 1200 Hz which covers both originate mode and the answer mode.

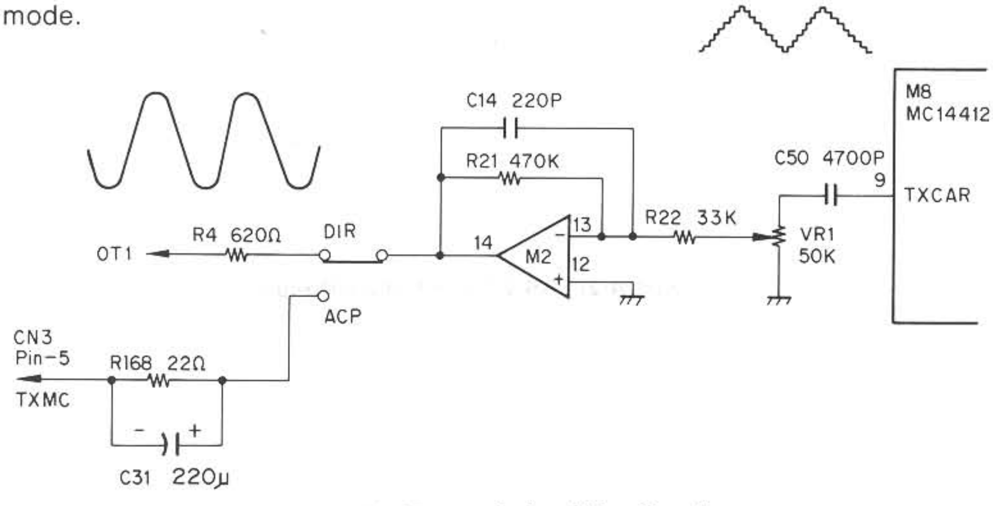


Figure 4-22. Transmission Filter Circuit

Reception Filter Circuit

As shown in Fig. 4-23, the reception input signal is amplified when passing through coupling capacitor (C11), and amplified again as it passes through the 3-stage band-pass filter (composed of an active filter). The signal then passes through the comparator, and after being changed to a square wave, is input at the RXCAR terminal of MC14412. Also, to check a carrier signal, this signal is input to the demultiplexer M23 as the CDD signal in the RS-232C interface circuit.

Intermediate frequencies of the 3-stage active filter are shown below. The switching of intermediate frequency for the originate and answer modes is accomplished by switching T1, T2 and T3 ON or OFF according to ORIG-ANS parameter in TELCOM mode, thus changing the input resistance of the filters.

On the other hand, three comparators consisting of M5 act as the carrier break down detector. The output of this circuit is "H" when a carrier signal has not been detected for the time specified by the C38 and R66.

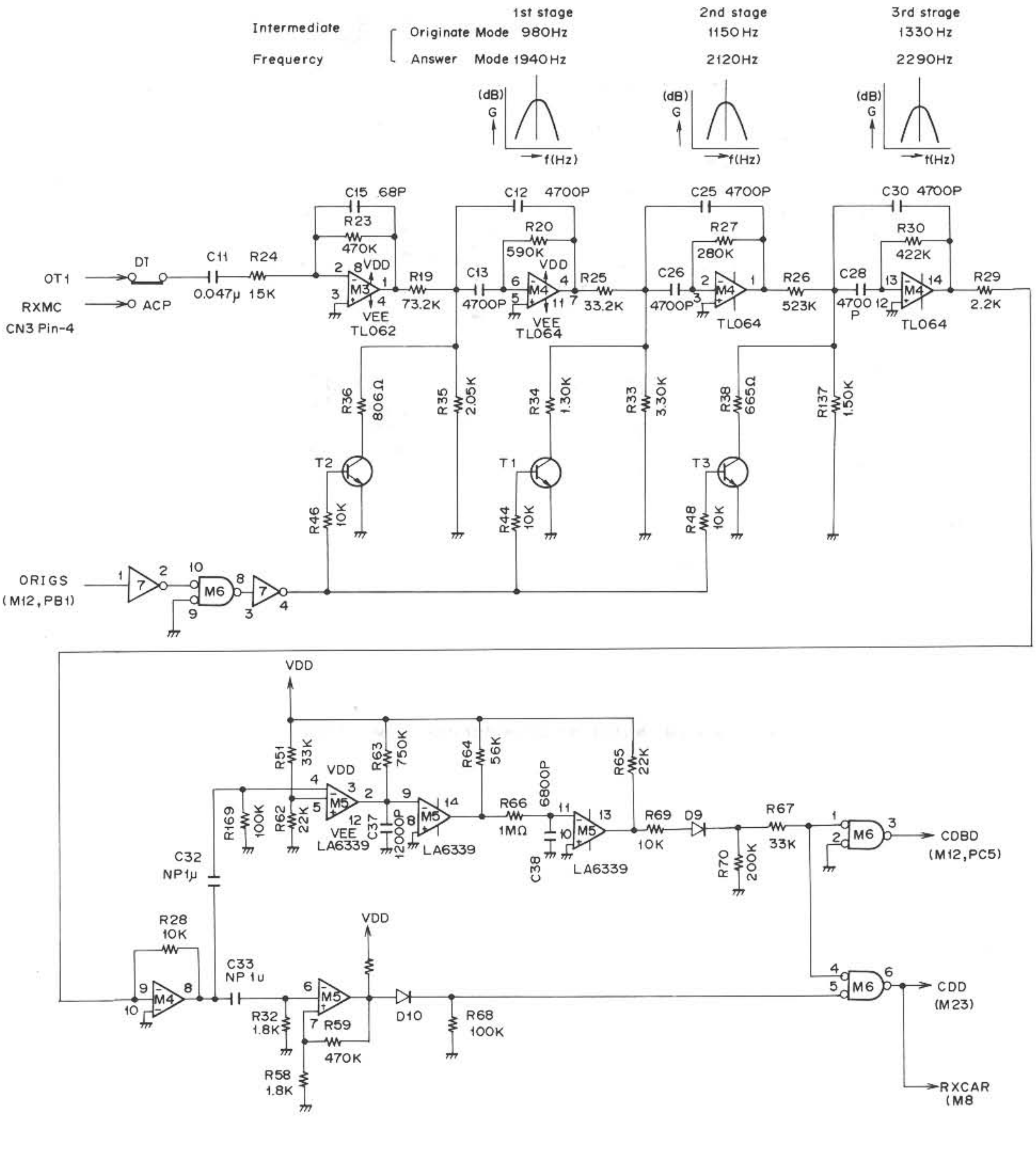


Figure 4-23. Reception Filter Circuit

MODEM Connector Interface Circuit

When the acoustic coupler is used, the transmission and reception signals are directly connected to the connector (TXMC, RXMC). When the MODEM cable is used, they are connected to the secondary side of the driver transformer. The primary side of this transformer is connected to the telephone line via the connector (TXMD, RXMD).
The ACP-DIR switch is used in the MODEM mode, relay RY2 separates the telephone receiver audio input signal (TL) to prevent interference. RY3, another relay, separates the modem circuit and the telephone at the conclusion of use in the MODEM mode and is also used as an automatic dialer for the pulse type telephone line.

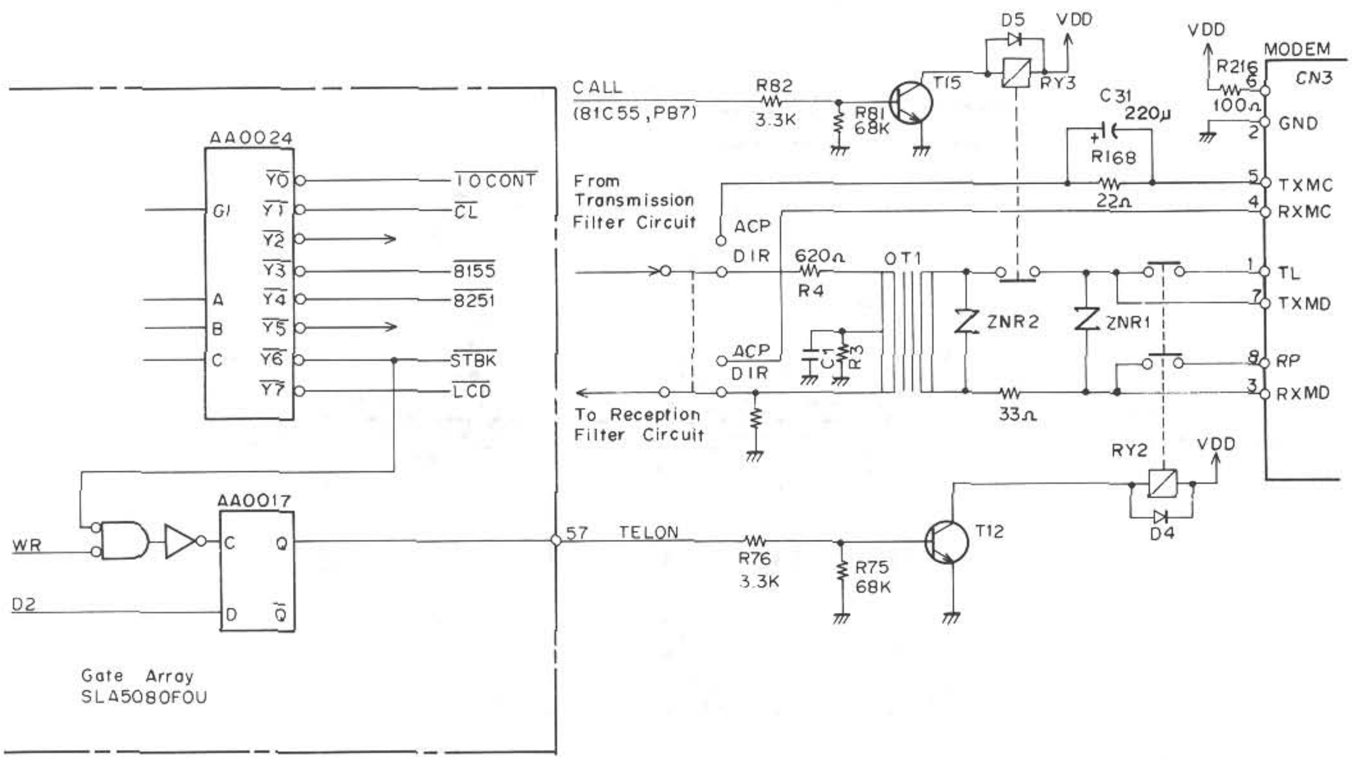


Figure 4-24. MODEM Connector Interface Circuit

Tone Signal Generator Circuit

The function of this circuit is to send tone-dial signals to the tone-type telephone line when the Tandy 200 is connected to that type of telephone line.

These functions described above are controlled by the IC TCM5089. The enable (TNE) signal input to this IC is created by NANDing the DTR signal and RS232C signal. That is, when the DTR signal becomes "H" during MODEM mode, this IC will be in the enable state.

Then the CPU writes the data to be dialed to the I/O port assigned by A0H – AFH.

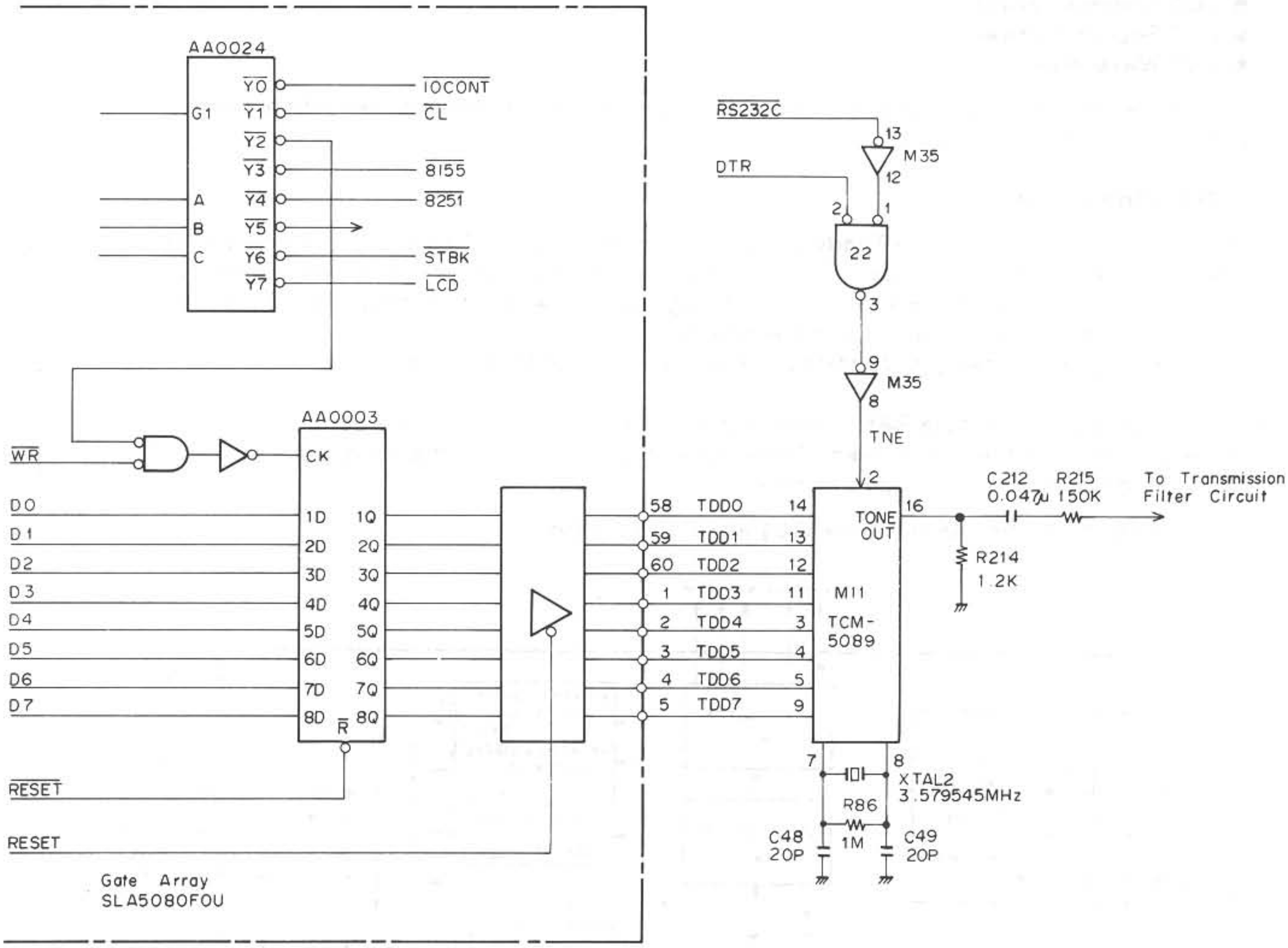


Figure 4-25. Tone Signal Generator Circuit

LCD

The LCD used in the Tandy 200 is composed of electrodes in a matrix arrangement (128 common signals and 480 segment signals). Refer to Figure 4-26.
Because this LCD operates on a 1/64-duty time division drive, the upper 64 and lower 64 common signals are performed by the same timing.
This part is subdivided into following four sections:

- **LCD Control Circuit**
- **LCD Common Driver**
- **LCD Segment Driver**
- **LCD Waveform**

For a more detailed description of how the LCD operates and its basic construction, refer to Appendix C of this manual.

LCD Control Circuit

The LCD Control Circuit of the Tandy 200 consists of the LCDC (HD61830B) and 8K-byte RAM.
The LCDC generates driving signals for LCD by receiving the instructions and data from the CPU.
The driving signals for LCD are divided into two groups: one is the timing signal for the segment driver and common driver, another is the data to display.
The CLKL signal, divided 2.4576 MHz clock signal by two at M34, is supplied to the RC terminal of the LCDC.
One bit value of the 8K-byte RAM connected to LCDC corresponds to one dot of illumination or non-illumination on the LCD screen. These data are converted into the serial data D1 and D2 at the LCDC, and then sent to the segment driver.

Figure 4-26 shows the internal block diagram of HD61830B.

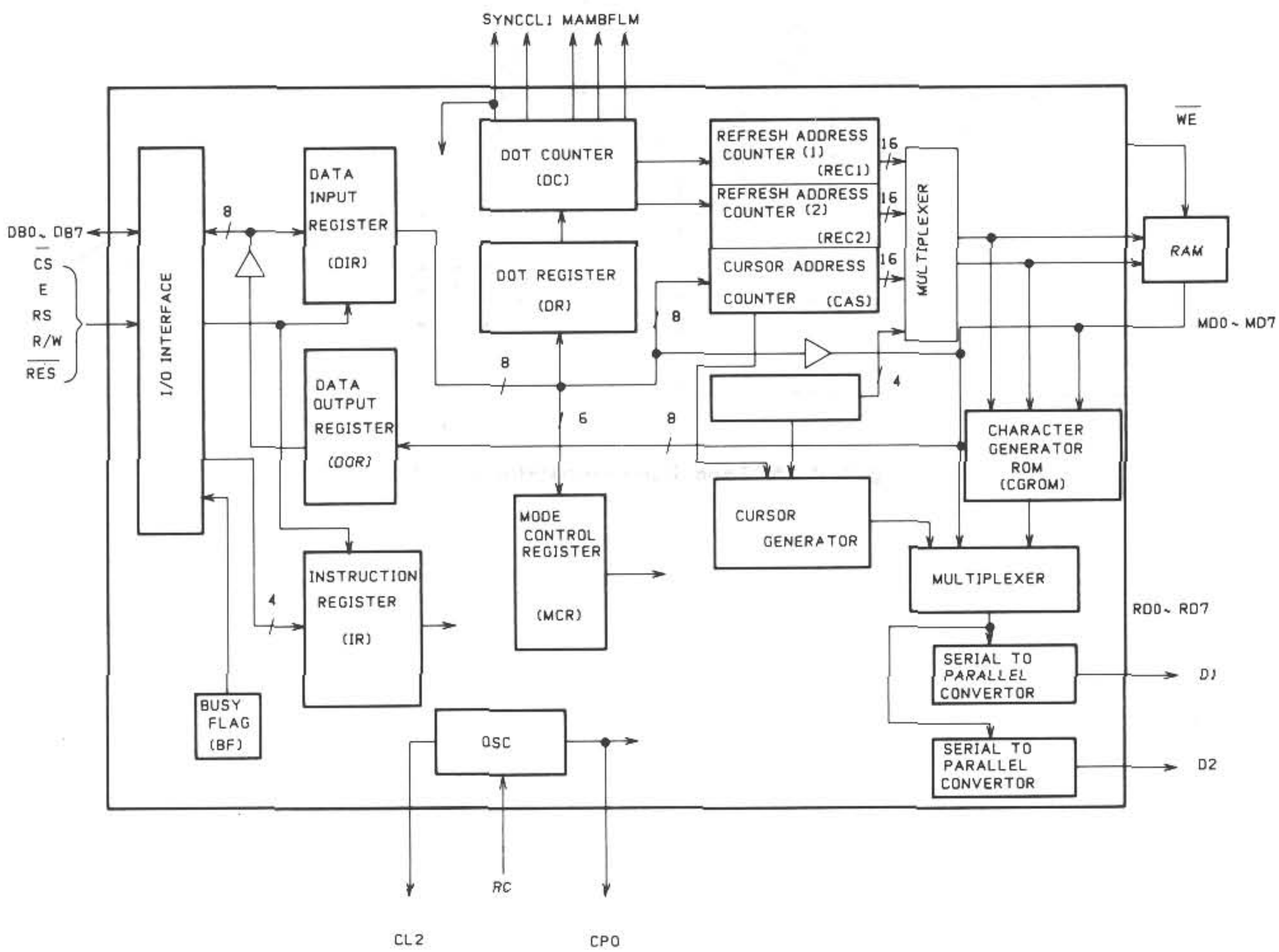


Figure 4-26. Internal Block diagram of HD61830B

The Common Driver (HD61103)

The Tandy 200 uses two common driver ICs: M507 and M508. M507 controls the upper half of the LCD screen and M508 controls the lower half of the LCD screen.
The FRM signal defines the periodic frequency of one-screen display, and determines 80 Hz for the Tandy 200.
The MB signal is used for changing the driver signal to AC. Because the continuous application of DC to the LCD would shorten the LCD element life.
The CL1 signal is used for the shift clock of the internal shift register.
Figures 4-27 and 4-28 show the internal block diagram of HD61103 and output waveform of HD61103.

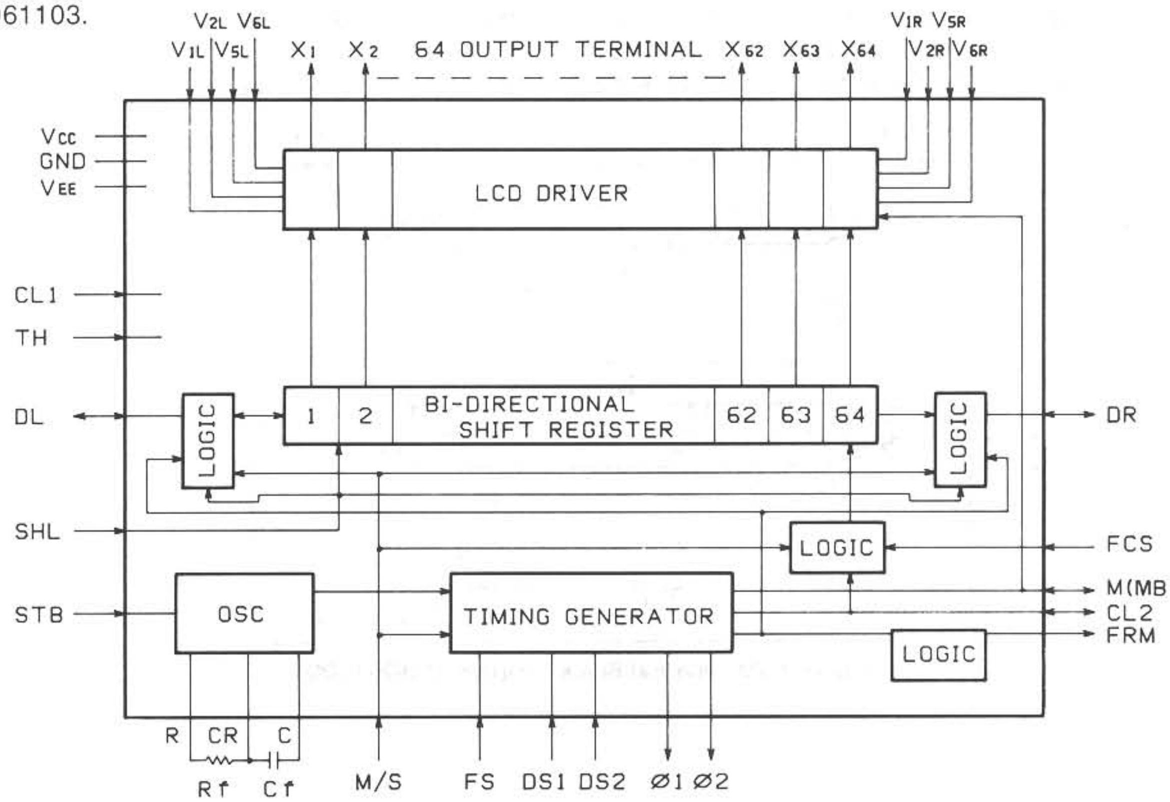


Figure 4-27. Internal Block Diagram of HD61103

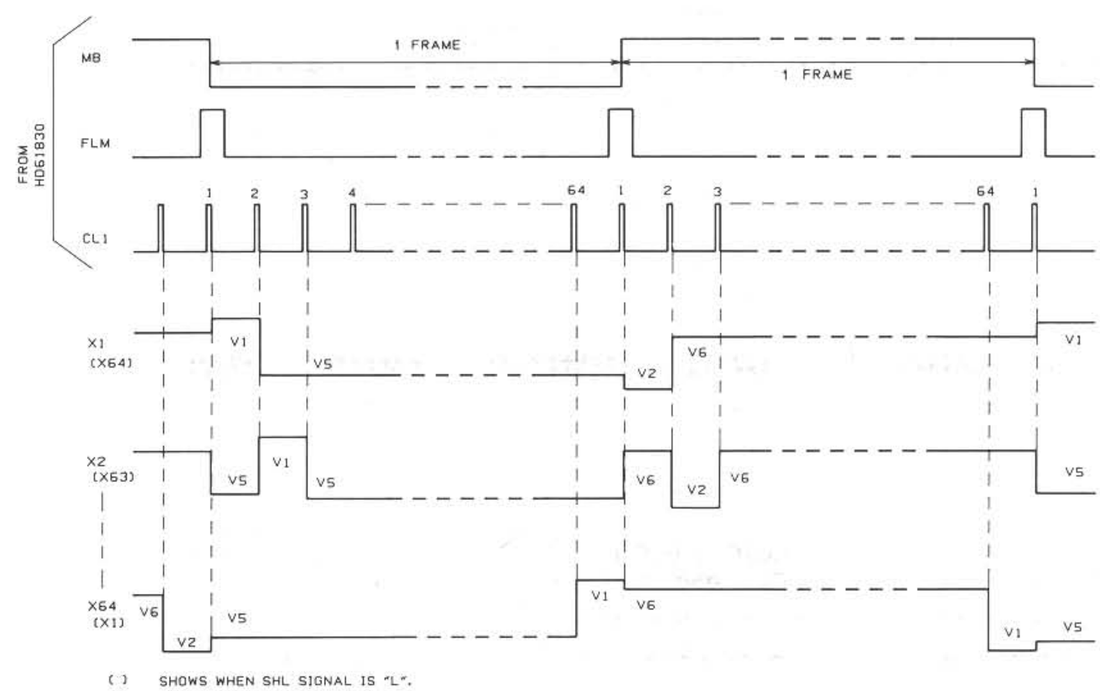


Figure 4-28. Output Waveform of HD61103

Segment Driver (HD61100)

The Tandy 200 uses six segment driver ICs(HD61100), and each IC has 80 output drivers.
HD61100 is a driver IC for the LCD display. It receives and latches the serial display data from the LCDC, and generates the segment driver signals.
The CL1, CL2, D1, D2 and MB signals are supplied from the LCDC. The CL1 signal is used for the latch clock of the internal 80 latches. Synchronizing with the fall of CL1, the segment driver signals corresponding to the display data are output.
The CL2 signal is used for the shift clock of the display data. The MB signal changes output signals to AC.
The D1 signal is the data to display on the upper half of the LCD screen and the D2 signal is the data to display on the lower half of the LCD screen.
Figures 4-29 and 4-30 show the internal block diagram of HD61100 and output waveform of HD61100.

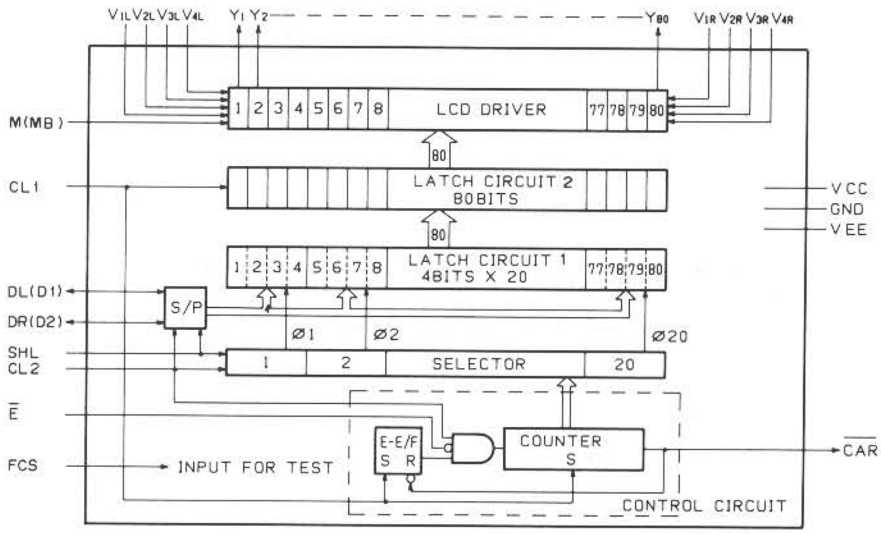


Figure 4-29. Internal Block Diagram of HD61100

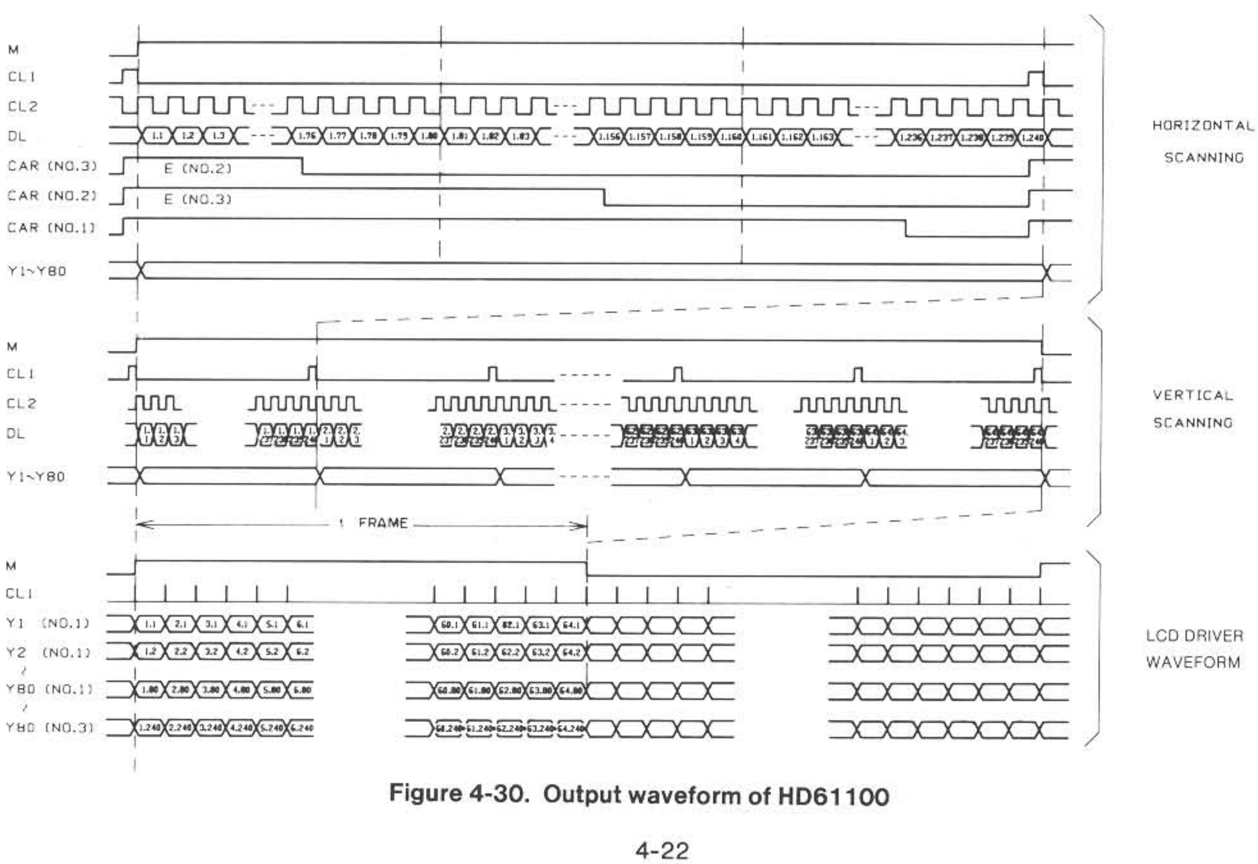


Figure 4-30. Output waveform of HD61100

LCD Waveform

In order to drive the liquid-crystal elements by the 1/64 duty line-sequential drive method, the LCD of the Tandy 200 makes sequential selection of the 64 scanning electrodes.
For each dot, the display signal passes through the signal electrodes and is applied 64 times for one display.
At this point, the signal is necessary at each dot only one time, and the signal for the other 63 times correspond to other dots on the same signal electrode.

The maximum voltage applied to the common electrode and segment electrode is the potential difference between V1 and V2.
In addition, "a" is the bias coefficient which determines from the standpoint of contrast, the maximum ratio between the illumination voltage and the non-illumination voltage.
When that ratio is greatest in relation to the effective ON and OFF voltages, "a"=9.0.
Thus, for V1, V2, V3, V4, V5 and V6:

V1=VDD(+5V)
V2=V0(approximately − 7V to − 10V)
V3=VDD − 2V/a
V4=VDD − (1 − 2/a)V
V5=VDD − (1 − 1/a)V
V6=VDD − V/a

Note: Absolute value of "V" equal absolute value of "VDD" plus absolute value of "V0".

Figure 4-31 shows the driving waveform for illumination and non-illumination.

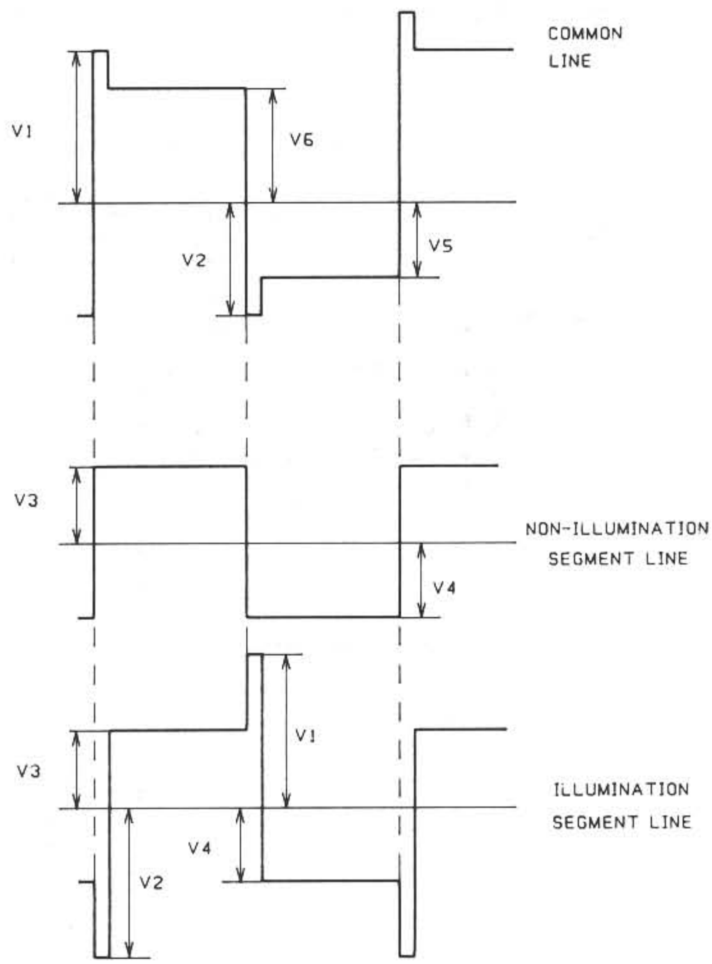


Figure 4-31. Driving Waveform of LCD

Power Supply and Auto-Power ON/OFF Circuit

The power supply circuit develops the following voltages:

- VDD (+5 volts DC)
- VEE (-5 volts DC)
- VLCD (-10 volts DC)
- VB
- VIN
- VD
- VR
- VNICD

VDD is supplied to all of the ICs except the main memory, TIMER (RP5C01), M24, M25 and M26.
VEE is used as a negative power source for the operational amplifiers.
VLCD is supplied to the LCD PCB through T27 for the LCD driving voltage.
VB is supplied to the main memory, TIMER, M24, M25 and M26.
VR is used for the input voltage to the DC/DC converter circuit. When the internal circuit is modified for use of Nickel-Cadmium batteries, VIN is supplied to the four Nickel-Cadmium batteries installed into the battery compartment.
This power source charges the Nickel-Cadmium batteries whenever an AC adapter is connected to the Tandy 200.

Power Distribution

Figure 4-32 shows the power distribution of the Tandy 200. In this circuit, R165 is used as the current limiter during the charge. D11 protects the power supply from the reverse current. The power control circuit controls the DC/DC converter circuit corresponding with the POWER, $\overline{\text{ALM}}$, PCS and BELL signals.

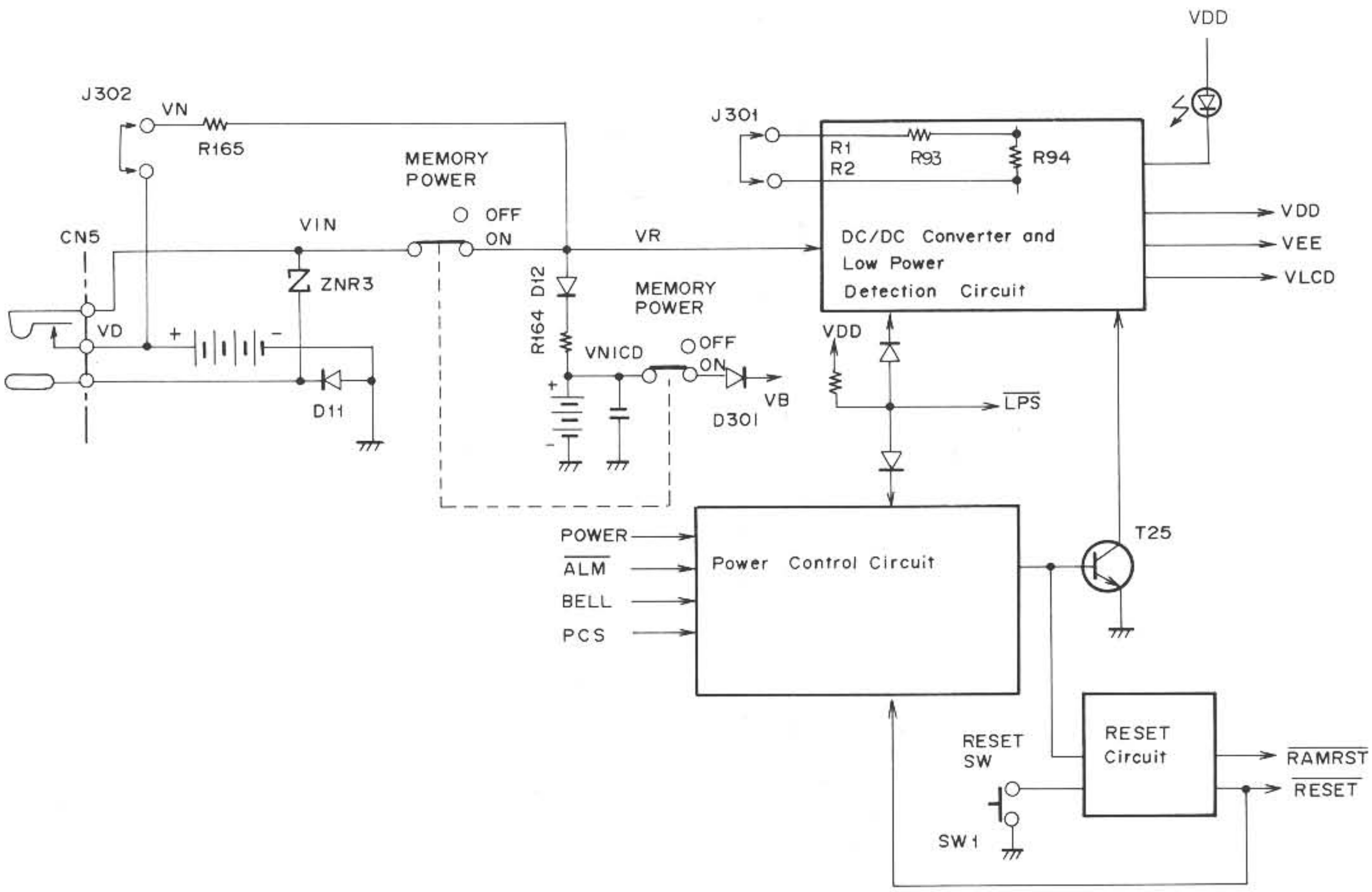


Figure 4-32. Power Distribution

DC/DC Converter

OT2 is a converter transformer which oscillates T20 and T21 and generates voltages at the secondary side of the transformer. At the same time the power is switched ON, a very slight collector current flows to T20 and T21. Also, voltage between pin 3 and pin 6 of the converter transformer is generated, and the T21 base potential becomes positive. In other words, the base polarity becomes biased in the forward direction. This voltage causes the T20 and T21 base current to flow, and the collector current is increased. When the current can no longer increase, because of transistor saturation and converter coil resistance, the voltage between pins 3 and 6 begins to attenuate, causing T20 and T21 to be cut off all at once because of the reverse playback action. Until immediately before the transistor is cut off, excitation current flows to the transformer. Because the current is suddenly dropped as a result of the transistor cut-off, a counter voltage is generated, the distributed capacity of the coil is changed, and, as a result, an oscillation voltage is generated at the base coil. Then, when the base potential progresses to a half cycle of the oscillation voltage, it is biased in the forward direction, T20 and T21 are switched ON once again. In this way, AC voltage corresponding to the number of windings is generated at the secondary side of the converter, and this voltage is rectified and smoothed by D13, D14, D15, C62, C63 and C64.

Low Power Detection Circuit

The low-power detection circuit illuminates an LED warning lamp when the battery voltage decreases. If it continues decreasing, the system power will be switched OFF just before the voltage becomes so low that the converter cannot operate.
There are about 20 minutes between the time when the LED lamp illuminates and the system is switched OFF.
Battery voltage is detected by splitting the resistance of R91, R92, R94 and R95. When battery voltage (VR) becomes 4.2V $\pm$0.1V, T18 is switched OFF. T19 is switched ON, T23 is driven, and the LED illuminates. (The LED is located on the keyboard PCB.)
In addition, the value of the detected voltage is changed by R93 because of difference between the output voltage of Alkaline-manganese and Nickel-Cadmium batteries.
The R1 and R2 signals are shorted on the memory PCB when the internal circuit is modified for use of Nickel-Cadminm batteries.

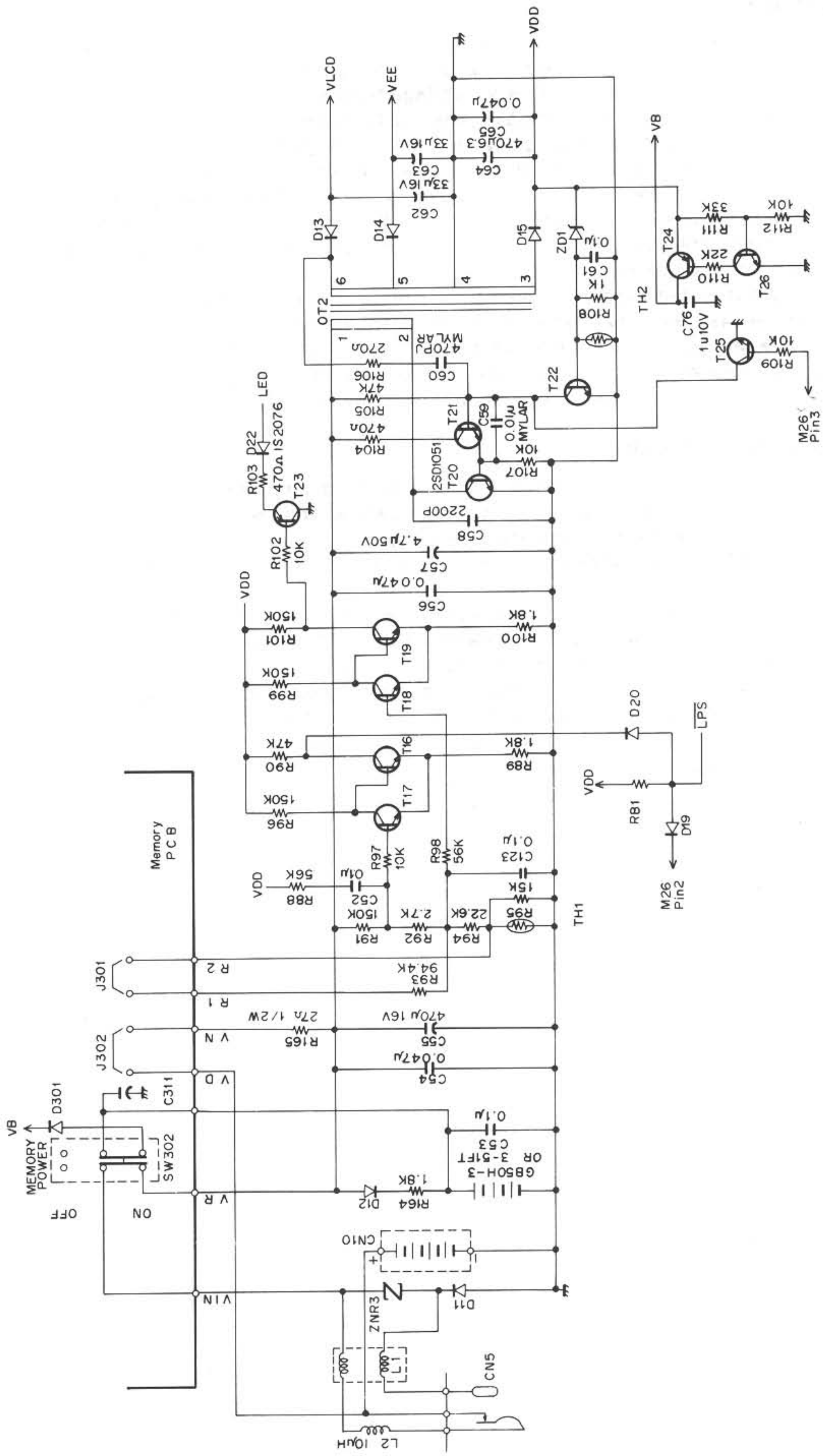


Figure 4-33. DC/DC Converter and Low Power Detection Circuit

Power Control Circuit

This circuit controls the oscillation of the DC/DC converter circuit by using T25. There are four methods to control the power ON/OFF. In this circuit, the VDD terminals of M24, M25 and M26 are connected to VB, since these ICs must operate in power-off condition.

1. Power-up using the POWER switch

If a customer presses the POWER switch on the keyboard during power-off condition, the following events occur:

a. A positive short pulse is sent to the base of T32 through C70, then T32 is switched on.

b. On the other hand, the BELL and $\overline{\text{RESET}}$ signals are "L" during power-off condition, but the input pin 8 of the gate M24 is pulled up to VB. Thus the output pin 10 of the gate M24 becomes "L," which enables the gate M25.

c. T31 is switched on. This "H" level signal is supplied to the RESET terminal of the flip-flop M26 and then the flip-flop M26 is reset.

d. The output pin 13 of the flip-flop M26 becomes "L" and T25 is switched off.

e. The DC/DC converter circuit starts the oscillation, if the proper DC level of VR is supplied to this circuit.

f. VDD reaches the specified DC level, T16 is switched off. At the same time, the $\overline{\text{LPS}}$ signal becomes "H" and is sent to the TRAP terminal of the CPU after inverted at M35.

g. When VDD reaches a constant DC level to operate the CPU, T28 is switched on and T29 is switched off. The $\overline{\text{RESET}}$ signal becomes "H," then the CPU begins the "Warm-Start" process. After completion of the "Warm-Start," the CPU drops the BELL signal.

h. The output pin 10 of the gate M24 becomes "H" and the output pin 10 of the gate M25 becomes "L", then the Tandy 200 will be able to operate.

2. Power-down using the POWER switch

If a customer presses the POWER switch on the keyboard during power-on condition, the following events occur:

a. A positive short pulse is sent to the base of the T32 through C70, and then T32 is switched on.

b. On the other hand, the cross-couple consisting of the gate M24 was set by the BELL signal in the last power-on sequence. Thus the output pin 11 of the gate M25 becomes "H."

c. The flip-flop M26 is clocked by this "H" level signal. The output pin 2 of flip-flop M26 becomes "L."

d. The LPS signal goes "L" and is sent to the TRAP terminal of the CPU after being inverted at M35.

e. This signal notifies the CPU when the customer presses the POWER switch. The CPU starts the internal power-down process. After completion of this process, the CPU sends the PCS signal passing through the PB of the 81C55.

f. Receiving the PCS signal, the output pin 4 of the gate M24 becomes "L."

g. The flip-flop M26 is set. The output pin 13 of M26 becomes "H" and T25 is switched on.

h. This causes the DC/DC converter to stop the oscillation. Then the Tandy 200 will not be able to operate.

3. Power-up using the $\overline{ALM}$ signal

The $\overline{ALM}$ signal becomes "L" when the time matches the value set by the POWER command in BASIC. The $\overline{ALM}$ signal is generated by the TIMER IC on the memory PCB. T31 is switched on by the "L" level $\overline{ALM}$ signal.
The remaining sequence follows the power-up using the POWER switch.

4. Power-down using the PCS signal

To control the power supply, the CPU sends the PCS signal if the automatic Power-Off limit reaches the value corresponding with the 1st parameter of the POWER command in BASIC.
The remaining sequence follows the Power-Down using the POWER switch.

Reset Circuit

This circuit supplies the CPU $\overline{RESET}$ signal and also the RAMRST signal as the RAM protecting signal when the power decreases. R113 and C66 delay the introduction of input power so that T28 is switched on and T29 is switched off after VDD is activated, with the result that the $\overline{RESET}$ signal changed from "L" to "H." In the same way, the RAMRST signal is generated by T30 and changes from "H" to "L." Thermistor TH3 suppresses the $\overline{RESET}$ signal fluctuations due to temperature. T27 receives the signal during automatic power OFF, short-circuiting both end of C66, and resets the system. The $\overline{RESET}$ signal is active "L" and the RAMRST signal is active "H."

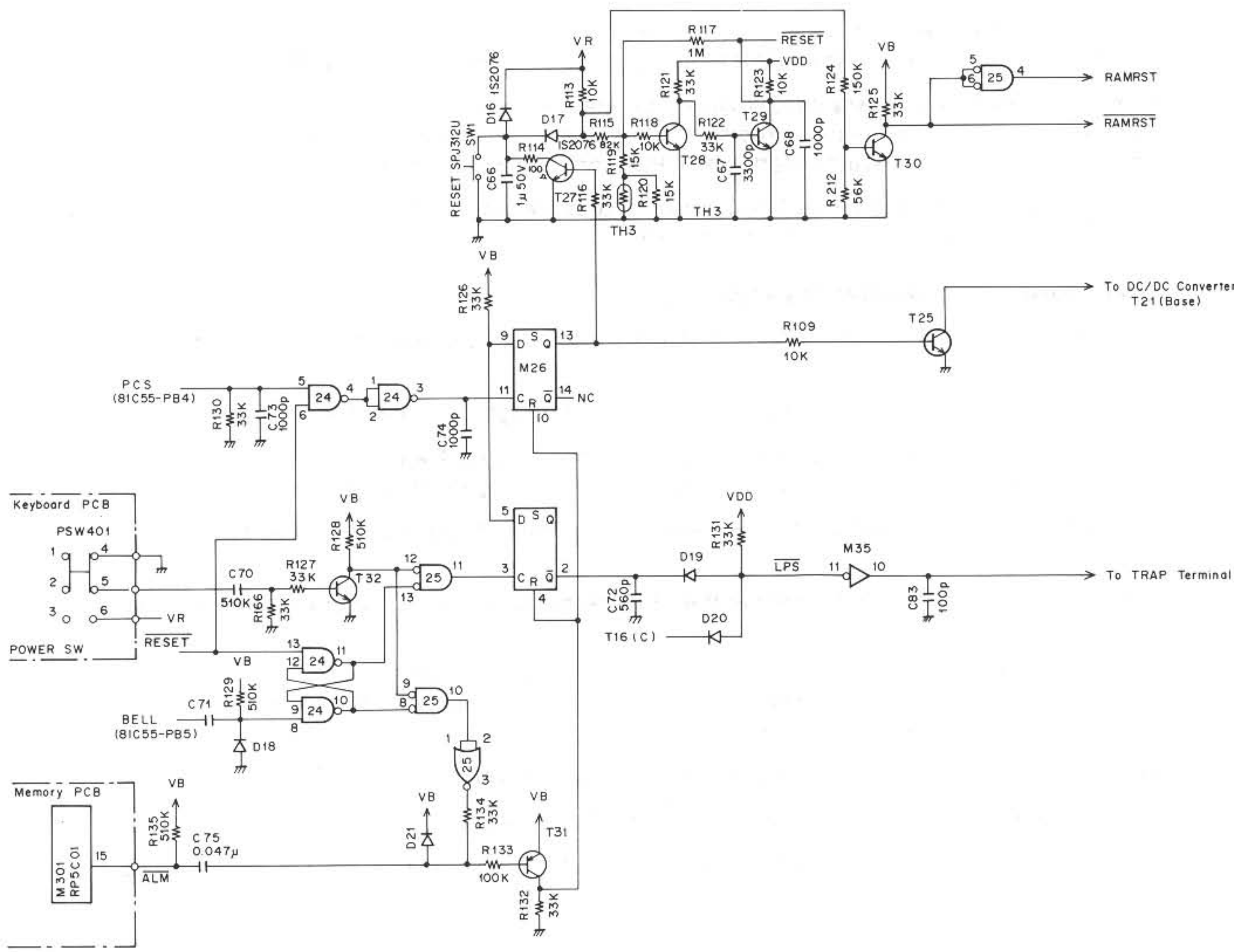


Figure 4-34. Power Control and Reset Circuit

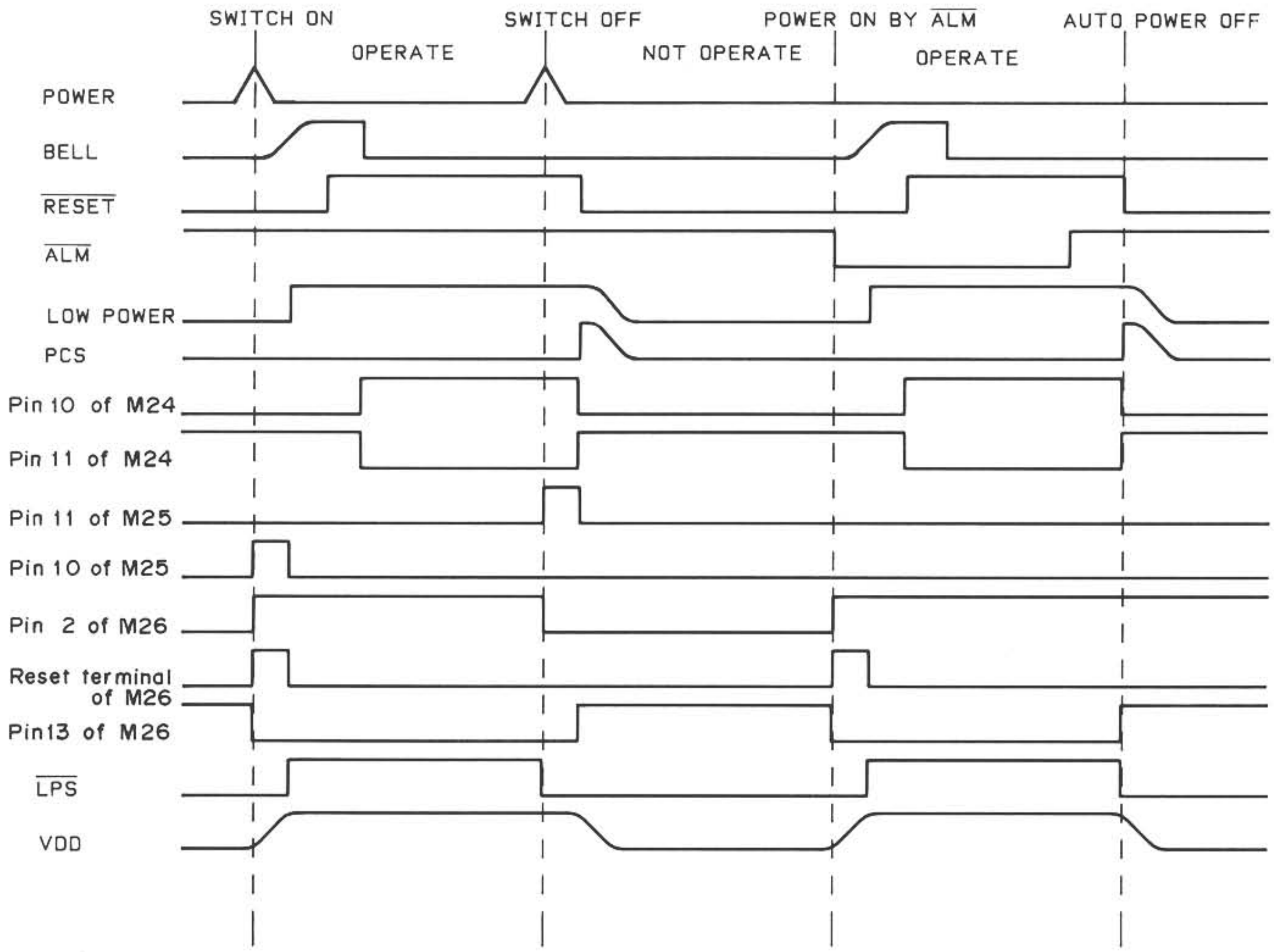


Figure 4-35. Power-Up/Down Sequence

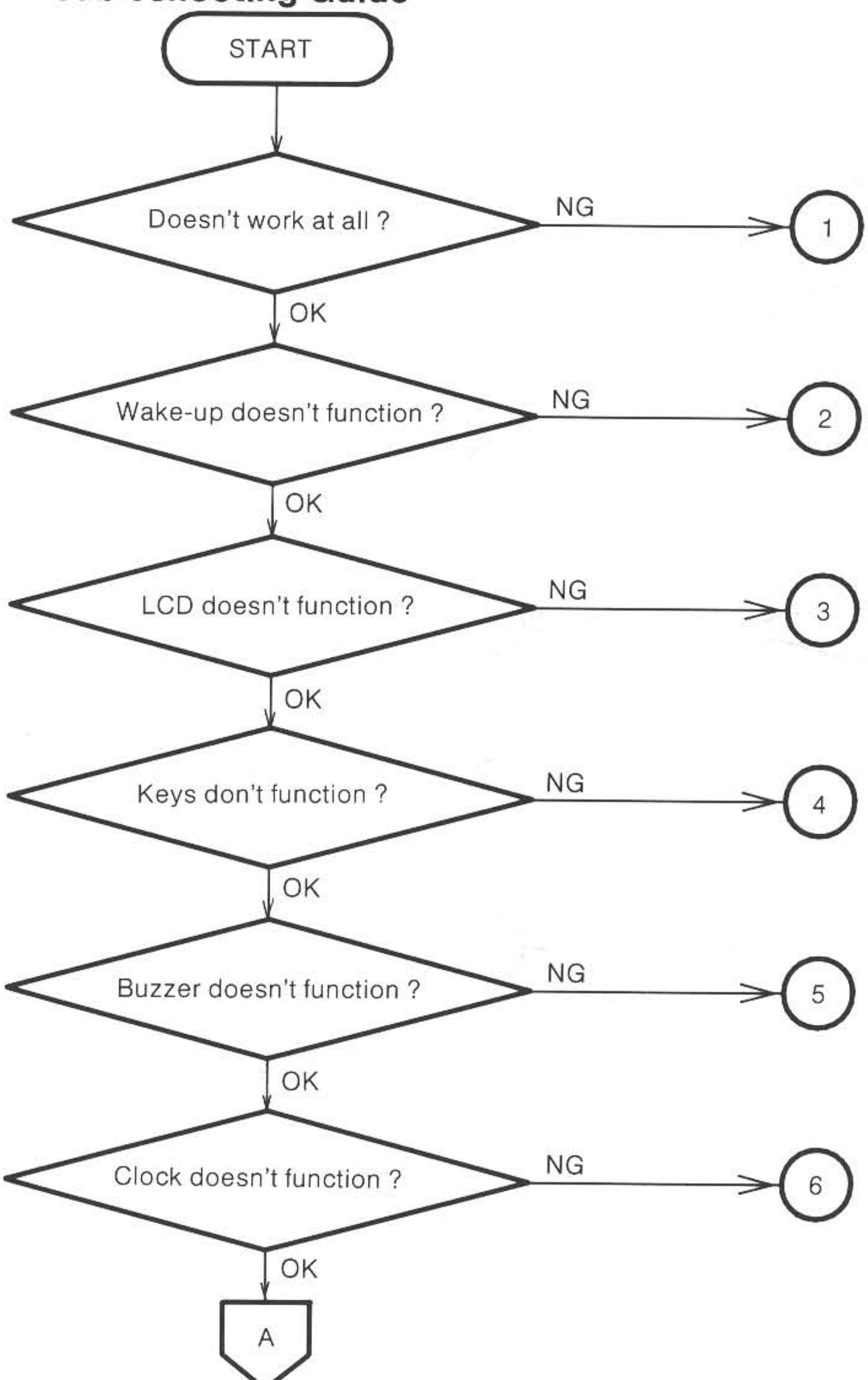
V. TROUBLESHOOTING

General Guidance

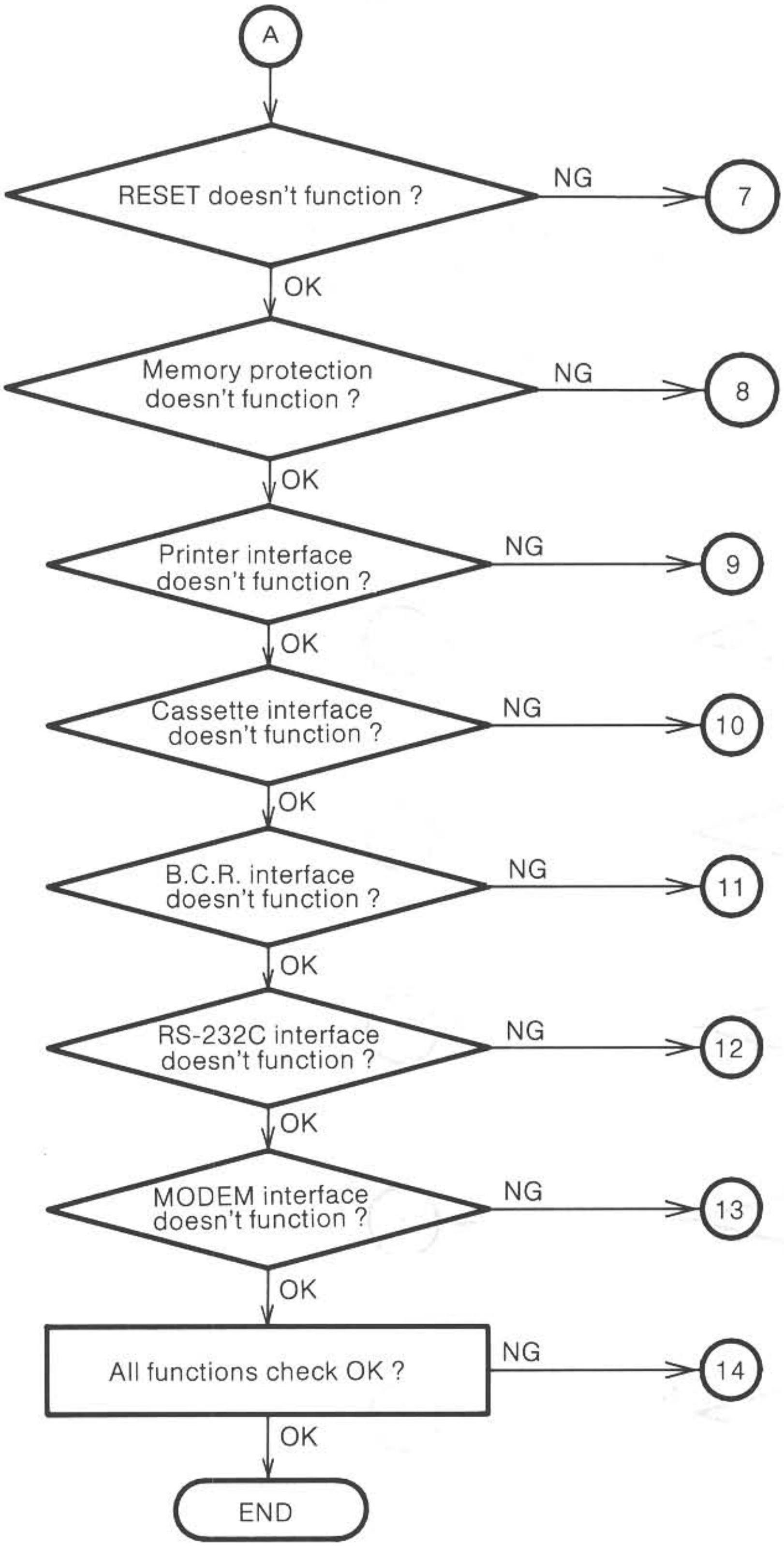
How to Make Use of This Section

If you have a problem or have to repair the Tandy 200, this section will be very helpful to you.
If the location or condition of the malfunctions are clear, for instance, buzzer does not function, refer to the flowchart in the Troubleshooting Guide and find the number circled. Then, you will be able to find necessary information such as corresponding IC's and transistors for malfunction repair.
After you complete malfunction repair, re-check each functional item according to the CHECK LIST.
You can make use of the CHECK LIST even if the location and condition of the malfunction are not clear.

Troubleshooting Guide



(to next page)


A
RESET doesn't function ?
NG
7
OK
Memory protection doesn't function ?
NG
8
OK
Printer interface doesn't function ?
NG
9
OK
Cassette interface doesn't function ?
NG
10
OK
B.C.R. interface doesn't function ?
NG
11
OK
RS-232C interface doesn't function ?
NG
12
OK
MODEM interface doesn't function ?
NG
13
OK
All functions check OK ?
NG
14
OK
END

Checking Procedure

1. Doesn't work at all

(1)

↓

Check the power
- Check to be sure that the batteries are in and that the AC adapter is connected.
- Is the memory back-up power switch ON ?
- Is the power switch ON ?

↓

Check the power ON-OFF circuit.
- Check C70, T32, M25, C71, D18, M24, T31 and M26.
- Check M25, M26, C72 and D19.

Check the DC/DC converter circuit.
- Is 3.6 – 8V applied to pin 1 of the converter transformer ?
  (If not, check C55, C54, battery contacts and adapter jack.)

Check all output voltages.
- a) VDD........ +5V (if not, check D15, C64 and ZD1)
- b) VEE .... –5V (if not, check D14 and C63)
- c) VLCD...... –10V (if not, check D13 and C62)
- d) VB........... +5V (if not, check T24 and T26)
  Is T20 oscillating ?
  (If not, check T21, T22, C60, R106, R105, R107 and T25)

↓

Check the $\overline{\text{LPS}}$ signal ?
- High level (+2.2V – 5.3V) ?
  (Check T16, T17, C52 and R88)
- Low level (0.8V – 0.3V) ?
  (Check M35)

↓

Check the $\overline{\text{RESET}}$ signal.
- Is it high level (+2.2V – 5.3V) ?
  If not, check T28, T29, T30 $\overline{\text{RESET}}$ signal.
- Is it low level (0.8V – 0.3V) ?
  If not, check T28, T29, T30, RESET signal.

↓

Check the logic circuit.
- Check the CPU clock frequency.
  (XTAL3 terminal = 4.9152 MHz; CLK terminal = 2.4576 MHz)
  (If not, check XTAL3 and M19.)
- Try replaceing the LCD unit.
- Check all IC's.

↓

END

2. Wake-up doesn't function

(2)

Check if Memory Board connector is correctly connected.

↓

Does $\overline{\text{ALM}}$ signal fall from "H" to "L" ?
M301 15pin ($\overline{\text{ALM}}$ sig), XTAL301, C306, C307, C75, D21, T31, M26

↓

END

3. LCD doesn't function

(3)

No display at all — NO: go to "Check the LCD waveform."

↓ YES

Check source voltage (VDD, VEE, VLCD, VB).
Refer to "1. Doesn't work at all".

↓

Check the $\overline{\text{RESET}}$ signal.
Refer to"7. Reset doesn't function".

↓

Check the LCD waveform.
(If abnormal, check the LCD power supply operation amplifier.)

↓

Check the interface circuitry.
M18 (HD61830B), M16 (8K-SRAM), T33, VR2, R136, and R137

↓

Check if connector is correctly connected.

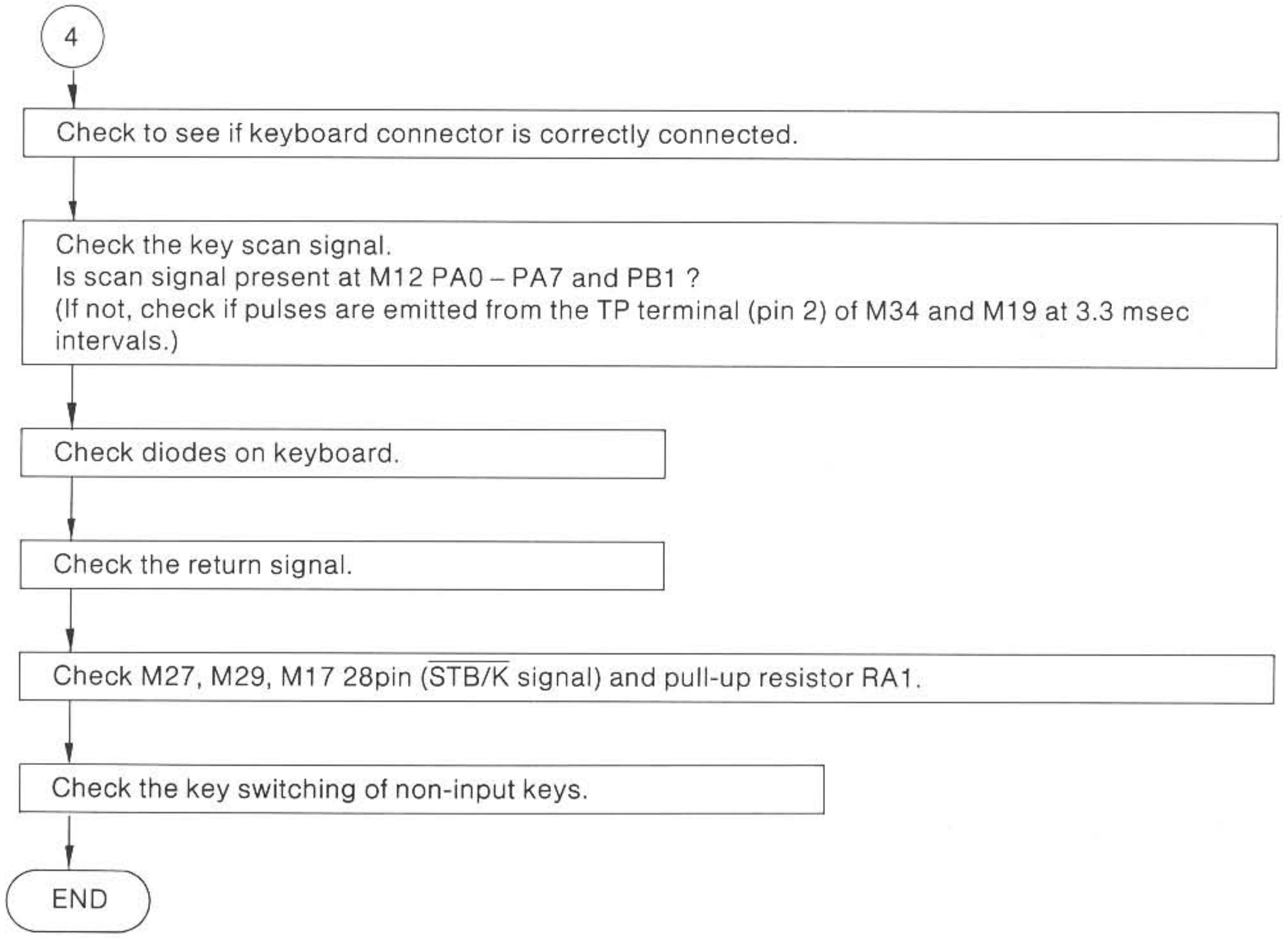
↓

Check LCD drivers (on LCD PCB) HD61100 and HD61103.
(Or replace the LCD unit.)

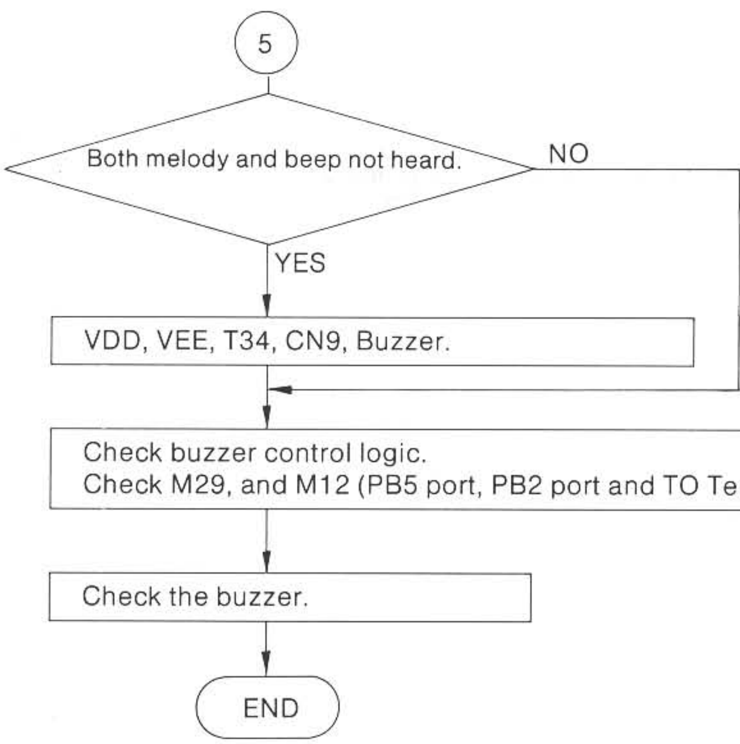
↓

END

4. Keys don't function



5. Buzzer doesn't function



6. Clock doesn't function

(6)

Check connector connections.
Check if MEMORY BOARD connector (CN 13) is correctly connected.

↓

Check the power supply voltage (VB).
- When power ON : +5V
- When power OFF: 3.0 – 4.0V

(If not normal, check power supply circuit.)

↓

Check oscillation frequency (32.768 kHz).
(If not normal, check XTAL301, C306, C307 and M301)

↓

Check clock-setting IC M12 and M17 (CL signal 31pin)

↓

(END)

7. Reset doesn't function

(7)

↓

Check RESET circuit.
(Check T28, T29, T30, T27, D16, D17 and C66)

↓

Check all ICs which have RESET and $\overline{\text{RESET}}$ signals.
(Check M19, M12, M20, M17, M25, M18 and M8, and also check LCD unit and RAM.)

↓

(END)

8. Memory protection doesn't function

(8)

↓

Check connector connections.
Check if MEMORY BOARD connector (CN 13) is correctly connected.

↓

Check power supply voltage.
When power ON : VB + 5V (if not, check converter circuit)
When power OFF: VB = 2.0 – 4.0V (if not, check Nickel-Cadmium batteries, D12 and D301)

↓

Check to be sure that there is no deviation in the timing of the signal and that the level changes symmetrically, when the RAMRST and RESET are switched ON/OFF.

↓

Check CMOS RAM.

↓

END

9. Printer interface doesn't function

(9)

↓

Check the strobe signals.
Check M9 and M17 (PSTB signal 6pin)

↓

Check the data signals.
Check M12, M9 and M10.

↓

Check the connector and printer cable.

↓

END

10. Cassette interface doesn't function

(10)

↓

Check TXC signals.
Is a modulated waveform output to pin 5 of the cassette connector during program or data save ?
(If not, check M1, M19, C2 and C3.)

↓

Check RXC signals.
Is a digital waveform input to the SID terminal of the CPU during program or data load ?
(If not, check D1, D2, M2, M1 and M19.)

↓

Check the remote circuit.
Check the relay (RY1), T11 and M17 (REMOTE sig. 56pin).

↓

Check the cassette connector and cassette cable.

↓

END

11. B.C.R. interface doesn't function

(11)

↓

Check M1, M12, and M19.

↓

Check the power supply voltage VDD (+5V).

↓

END

12. RS-232C interface doesn't function

(12)

↓

Check transmit side.
Check if the switching digital signal (± 5V – ± 3.5V) is output to connector pin 2 during transmission. Then check if the CTS signal of pin 5 is low level.
(If not output, check M20, M22, M35, M21 and M12 (PB3 port).

↓

Check receive side.
Check if a digital signal is input to M20 pin 3 (RXD terminal) during data reception.
(If not emitted, check M20, M33, M23, D23, D24 and D25).

↓

Check the RS-232C select signal.
Check if PB3 port (pin 32) of M12 is low level.
(If not, check M12 and M35.)

↓

Check RS-232C connector and cable.

↓

END

13. MODEM interface doesn't function

(13)

↓

Check transmit side.
Check if a modulation signal is output to connector pin 5 (during coupler mode) or pin 7 (during direct mode) during transmission. Then check if the receiver carrier is input to the M8 RX CAR terminal (pin 1).
(If not, check M20, M2, T15, OT1 and RY3.)

↓

Check receive side.
Check to be sure that the modulation signal is input to M8 pin 1 (RX CAR) during data reception.
(If not, check M3, M4, OT1, T1, T2, T3, T9 and RY3. If it is input, check M20.)

↓

Check the automatic pulse dialer.
Check RY2, RY3, T12, T15, M12 (PB7 port) and M17 (TELON sig. 57pin).

↓

Check the automatic tone dialer.
Check M11, XTAL2, R86, C48, C49, M17 (TDD0-TDD7 signal)
OT1, RY2, RY3, T12, T15, M12 (PB7 port), M17 (TELON sig. 57pin) M35, M22 and M20.

↓

(END)

14. Check system again

(14)

↓

Check unit again as described in the Troubleshooting Guide.

Check List

After completing all repairs and adjustment, check all functions according to the Test Program as shown below. Before beginning the checking, initialize the RAM contents by performing a cold start. Refer to "(5) Reset function test".

(1) Wake-up check (in BASIC mode)
   10 TIME$ = "00 : 00 : 55"
   20 POWER "00 : 01 : 00"
   30 POWER OFF
   After executing above program, it will be powered OFF and then powered ON after five seconds.

(2) Buzzer and LCD check (in BASIC mode)
   10 FOR I = 0 TO 255
   20 PRINT CHR$ (I);
   30 NEXT I
   40 END
   Operation
   After 1 beep and the LCD display clears, all characters are displayed.

(3) Clock test (in BASIC mode)
   (a) Setting the year, month, date, day, hour and second:
      Year, month, date setting: DATE$ = "MM/dd/YY"
      Day setting: DAY$ = "day" (example:Sunday = SUN)
      Hour, minute, scond setting: TIME$ = "HH: MM: SS"
   (b) Confirmation of set data
      Return to menu executing MENU command, and then check to be sure that the calendar data changes to set data.

(4) Keyboard test
   Refer to character code table in the Appendix B and check that all keys are input.

(5) Reset function test (memory protection test)
   (a) Warm start
      Press the RESET switch on the rear of the case or switch the POWER switch to ON, and check that initialization is made. Also check, however that the saved USER files are not erased.
   (b) Cold start
      While pressing the CTRL and PAUSE keys, press the RESET switch and check that all USER files are initalized.

(6) Printer interface test (in BASIC mode)
   Input the characters to be printed out on the LCD display, and then, when the hard copy key PRINT is pressed, the displayed characters will all be printed out.

(7) Cassette interface test (in BASIC mode)
   Input a suitable program, save it on cassette (by CSAVE "file name"), and then read out the saved program (by CLOAD "file name") and check it.

(8) For the RS-232C and MODEM tests, prepare two units and make the tests while referring to the section concerning communications in the Operation Manual.

VI. PARTS LIST/ EXPLODED VIEW

Exploded View

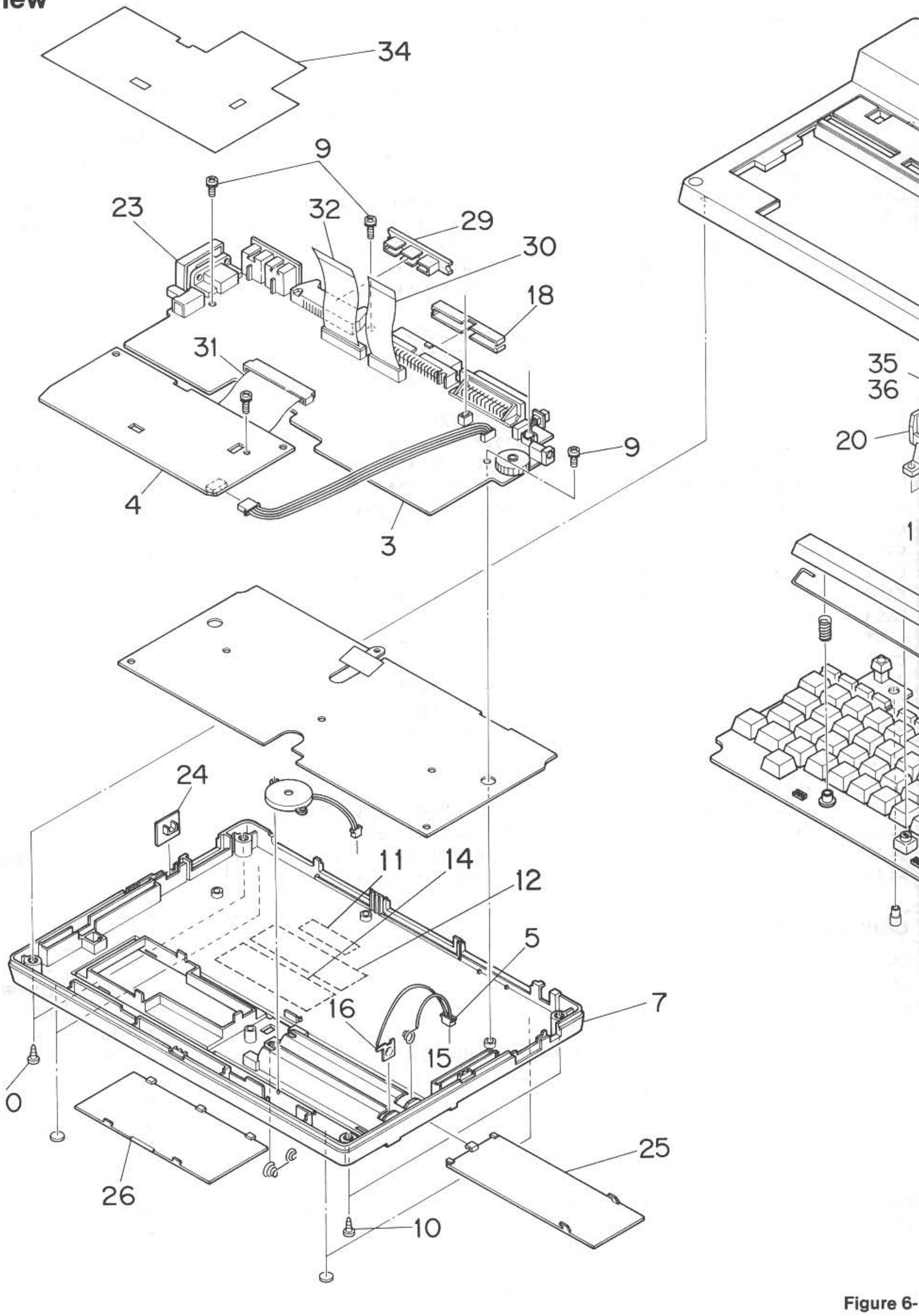


Figure 6-

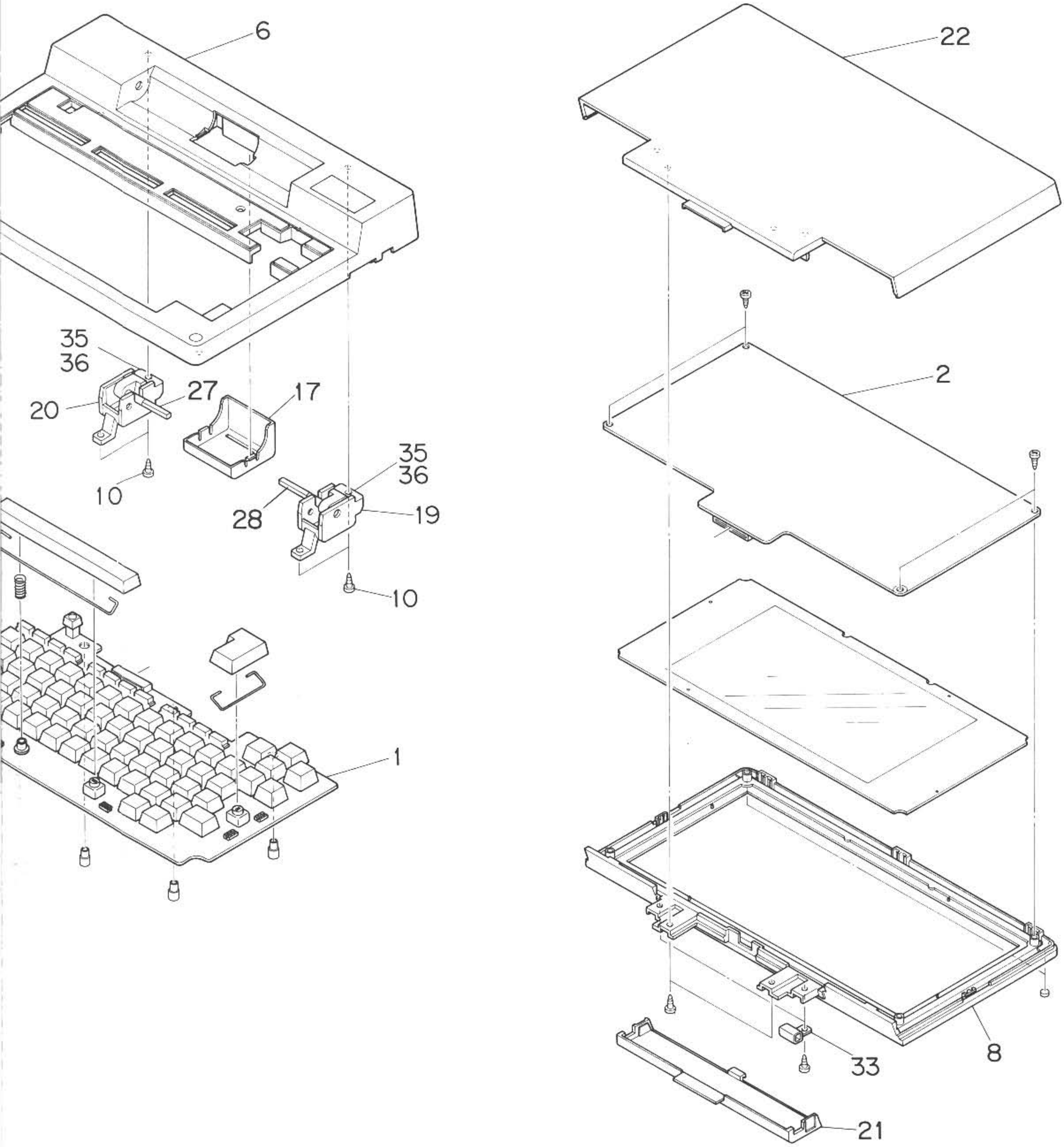


Figure 6-1. Exploded View

Ref. No.	Description	RS Part No.	Mfr's Part No.
C66	Capacitor, Electrolytic 1μF/50V/±20%		CEVG010ALN
C67	Capacitor, Ceramic 3300pF/50V/±10%		CFPD332KB%
C68	Capacitor, Ceramic 1000pF/50V/±10%		CFPD102KB%
C69	Not used		
C70	Capacitor, Ceramic 560pF/50V/±10%	CD-561KJCP	CFPD561KP%
C71	Capacitor, Ceramic 0.047μF/50V/+80 -20%		CFPD473ZF%
C72	Capacitor, Ceramic 560pF/50V/±10%	CD-561KJCP	CFPD561KP%
C73	Capacitor, Ceramic 1000pF/50V/±10%		CFPD102KB%
C74	Capacitor, Ceramic 1000pF/50V/±10%		CFPD102KB%
C75	Capacitor, Ceramic 0.047μF/50V/+80 -20%		CFPD473ZF%
C76	Capacitor, Tantalum 1μF/10V/±20%		CSPC010MLN
C77	Capacitor, Ceramic 0.01μF/50V/±10%		CFPD103KB%
C78	Capacitor, Ceramic 10pF/50V/±0.5%		CFPD100DC%
C79	Capacitor, Ceramic 10pF/50V/±0.5%		CFPD100DC%
C80	Not used		
C81	Capacitor, Electrolytic 33μF/16V/±20%		CEVD330ALN
C82	Capacitor, Ceramic 100pF/50V/±10%		CFPD101K0%
C83	Capacitor, Ceramic 1000pF/50V/±10%		CFPD102KB%
C84	Not used		
C85	Capacitor, Ceramic 0.1μF/25V/+80 -20%		CFPC104ZF%
C86	Capacitor, Mylar 0.039μF/50V/±5%		CQVB393JTN
C87	Capacitor, Mylar 0.039μF/50V/±5%		CQVB393JTN
C88	Capacitor, Mylar 0.039μF/50V/±5%		CQVB393JTN
C89-C99	Capacitor, Ceramic 0.1μF/25V/+80 -20%		CFPC104ZF%
C100	Not used		
C101	Not used		
C102	Capacitor, Ceramic 0.1μF/25V/+80 -20%		CFPC104ZF%
C103	Capacitor, Ceramic 100pF/50V/±10%		CFPD101K0%
C104	Not used		
C105	Capacitor, Tantalum 10μF/6.3V/±20%		CSPB100MLN
C106	Not used		
C107	Capacitor, Tantalum 10μF/6.3V/±20%		CSPB100MLN
C108	Capacitor, Tantalum 10μF/6.3V/±20%		CSPB100MLN
C109 ~ C118	Capacitor, Ceramic 33pF/50V/±10%		CFPD330KP%
C119	Not used		
C120	Capacitor, Ceramic 0.1μF/25V/+80 -20%		CFPC104ZF%
C121	Capacitor, Ceramic 0.1μF/25V/+80 -20%		CFPC104ZF%
C122	Capacitor, Mylar 0.047μF/50V/+80 -20%		CQVB473JTN
C123	Capacitor, Ceramic 0.1μF/25V/+80 -20%		CFPC104ZF%
CONNECTORS			
CN1	Jack, Junction to BCR		YJF09S039Z
CN2	Jack, Junction to CMT		YJF08S033Z
CN3	Jack, Junction to Modem		YJF08S034Z
CN4	Jack, Junction to Printer	AJ-7632	YJF26S011Z
CN5	Jack, Junction to AC Adapter - HEC 0470	AJ-7627	YJB03S007Z
CN6	Jack, Junction to System Bus	AJ-7634	YJF40S013Z
CN7	Jack, Junction to LCD	AJ-7629	YJF10S066Z
CN8	Jack, Junction to RS-232C	AJ-7631	YJF25S019Z
CN9	Jack, Junction to Buzzer	AJ-7628	YJF02S077Z
CN10	Jack, Junction to LED		YJF02S041Z
CN11	Not used		
CN12	Jack, Junction to Keyboard	AJ-7630	YJF22S015Z
CN13	Jack, Junction to Memory PCB	AJ-7633	YJF40S012Z
CN14	Connector and Cord Ass'y, to Memory PCB	AW-3266	ACCNM08GEA

Main PCB Assembly

Ref. No.	Description		RS Part No.	Mfr's Part No.
CAPACITORS				
C1	Capacitor, Mylar*	5600pF/50V/±5%		CQVB562JTN
C2	Capacitor, Mylar	0.047µF/50V/±5%		CQVB473JTN
C3	Capacitor, Mylar	0.1µF/50V/±5%		CQVB104JTN
C4	Capacitor, Ceramic	0.047µF/50V/+80 -20%		CFPD473ZF%
C5	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C6	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C7	Not used			
C8	Not used			
C9	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C10	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C11	Capacitor, Mylar	0.047µF/50V/±5%		CQVB473JTN
C12	Capacitor, Poly Film	4700pF/100V/±1%		CQPC472FEN
C13	Capacitor, Poly Film	4700pF/100V/±1%		CQPC472FEN
C14	Capacitor, Ceramic	220pF/50V/±10%	CD-221KJCP	CFPD221KB%
C15	Capacitor, Ceramic	68pF/50V/±10%	CD-680KJCP	CFPD680K0%
C16-C24	Not used			
C25	Capacitor, Poly Film	4700pF/100V/±1%		CQPC472FEN
C26	Capacitor, Poly Film	4700pF/100V/±1%		CQPC472FEN
C27	Not used			
C28	Capacitor, Poly Film	4700pF/100V/±1%		CQPC472FEN
C29	Not used			
C30	Capacitor, Poly Film	4700pF/100V/±1%		CQPC472FEN
C31	Capacitor, Electrolytic	220µF/16V/±20%		CEVD221ALN
C32	Capacitor, Electrolytic	1µF/50V/±20%		CEVG010NLX
C33	Capacitor, Electrolytic	1µF/50V/±20%		CEVG010NLX
C34	Not used			
C35	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C36	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C37	Capacitor, Ceramic	0.012µF/50V/±10%	CD-123KJCP	CFPD123KB%
C38	Capacitor, Ceramic	6800pF/50V/+80 -20%		CFPD682ZF%
C39	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C40	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C41	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C42	Capacitor, Ceramic	0.047µF/50V/+80 -20%		CFPD473ZF%
C43	Not used			
C44	Not used			
C45	Capacitor, Ceramic	0.047µF/50V/+80 -20%		CFPD473ZF%
C46	Capacitor, Ceramic	0.047µF/50V/+80 -20%		CFPD473ZF%
C47	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C48	Capacitor, Ceramic	20pF/50V/±10%		CFPD200KP%
C49	Capacitor, Ceramic	20pF/50V/±10%		CFPD200KP%
C50	Capacitor, Poly Film	4700pF/100V/±1%		CQPC472FEN
C51	Not used			
C52	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C53	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C54	Capacitor, Ceramic	0.047µF/50V/+80 -20%		CFPD473ZF%
C55	Capacitor, Electrolytic	470µF/16V/±20%		CEVD471UMN
C56	Capacitor, Ceramic	0.047µF/50V/+80 -20%		CFPD473ZF%
C57	Not used			
C58	Not used			
C59	Capacitor, Mylar	0.01µF/50V/±5%		CQVB103JTN
C60	Capacitor, Poly Film	470pF/100V/±5%	CC-471JLGP	CQPC471JTN
C61	Capacitor, Ceramic	0.1µF/25V/+80 -20%		CFPC104ZF%
C62	Capacitor, Electrolytic	33µF/16V/±20%		CEVD330ALN
C63	Capacitor, Electrolytic	33µF/16V/±20%		CEVD330ALN
C64	Capacitor, Electrolytic	470µF/6.3V/±20%		CEVB471ALN
C65	Capacitor, Electrolytic	0.047µF/50V/+80 -20%		CFPD473ZF%

* Mylar is a registered trademark of E. I. Du Pont de Nemours and Company.

Ref. No.	Description		RS Part No.	Mfr's Part No.
DIODES				
D1~D5	Diode, Silicon, 1S2076			QDSS2076#B
D6	Not used			
D7	Not used			
D8	Diode, Silicon, 1S2076			QDSS2076#B
D9	Diode, Silicon, 1S2076			QDSS2076#B
D10	Diode, Silicon, 1S2076			QDSS2076#B
D11	Diode, Silicon, ERA81-004			QDS81004XZ
D12	Diode, Silicon, 1S2076			QDSS2076#B
D13	Diode, Silicon, ERA81-004			QDS81004XZ
D14	Diode, Silicon, ERA81-004			QDS81004XZ
D15	Diode, Silicon, ERA81-004			QDS81004XZ
D16~D25	Diode, Silicon, 1S2076			QDSS2076#B
COILS				
L1	Coil, Troidal, SNH13-0401-2			LWD700101A
L2	Not used			
L3	Coil, RF, BP53BH3510045BA			LBADG5205A
L4	Coil, RF, BP53BH3510045BA			LBADG5205A
L5	Coil, RF, BP53BH3510045BA			LBADG5205A
INTEGRATED CIRCUITS				
M1	IC, C-MOS, Schmitt Trigger	HD14584BFP		QQF14584AB
M2	IC, Bipolar, Op-Amp.	TL064		QQF00064AU
M3	IC, Bipolar, Op-Amp.	TL062		QQF00062AU
M4	IC, Bipolar, Op-Amp.	TL064		QQF00064AU
M5	IC, Bipolar, Comparator	LA6339M		QQF06339AC
M6	IC, Hi-speed C-MOS, OR Gate	TC40H032F		QQF40032AT
M7	IC, Hi-speed C-MOS, Inverter	TC40H004F		QQF40004AT
M8	IC, C-MOS, Modem	MC14412VP	AMX-5808	QQ014412AM
M9	IC, Hi-speed C-MOS, Buffer	TC40H367F		QQF40367AT
M10	IC, Hi-speed C-MOS, Buffer	TC40H367F		QQF40367AT
M11	IC, C-MOS, Tone Dialer	TCM5089	MX-6491	QQ005089AU
M12	IC, C-MOS, PIO	MSM81C55RS		QQ008155A5
M13	IC, C-MOS, ROM	HM61364 or	MX-6485	QQ061364BB
		SMM2365		QQ002365AZ
M14	IC, C-MOS, ROM	HN613256P or	MX-6484	QQ061325SB
		SMM2326		QQ002326BZ
M15	IC, C-MOS, ROM	HN613256 or	MX-6483	QQ061325RB
		SMM2326		QQ002326AZ
M16	IC, C-MOS, RAM	HM6264P-15	MX-6481	QQ006264BB
M17	IC, C-MOS, Gate Array	SL5080FOU	MX-6479	QQF05080AZ
M18	IC, C-MOS, LCD Driver	HD61830B	MX-6480	QQF61830AB
M19	IC, C-MOS, CPU	MSM80C85ARS	AMX-5806	QQ008085A5
M20	IC, C-MOS, USART	MSM82C51ARS	MX-6482	QQ008251A5
M21	IC, C-MOS, Schmitt Trigger	HD14584BFP		QQF14584AB
M22	IC, Hi-speed C-MOS, OR Gate	TC40H032F		QQF40032AT
M23	IC, Hi-speed C-MOS, Selector	TC40H157F		QQF40157AT
M24	IC, C-MOS, NAND Gate	TC4011F or	MX-5444	QQF04011BT
		MN4011BS or		QQF04011AN
		HD14011BFP		QQF04011CB
M25	IC, C-MOS, NAND Gate	TC4001F or		QQF04001BT
		MN4001BS or		QQF04001AN
		HD14001BFP		QQF04001CB

Ref. No.	Description		RS Part No.	Mfr's Part No.
M26	IC, C-MOS, D-Flip-Flop	TC4013F or		QQF04013BT
		MN4013BS or		QQF04013AN
		HD14013BFP		QQF04013CB
M27	IC, Hi-speed C-MOS, Buffer	TC40H245F		QQF40245AT
M28	Not used			
M29	IC, Hi-speed C-MOS, OR Gate	TC40H032F		QQF40032AT
M30	IC, Hi-speed C-MOS, Buffer	TC40H367F		QQF40367AT
M31	Not used			
M32	IC, Hi-speed C-MOS, Buffer	TC40H367F		QQF40367AT
M33	IC, C-MOS, Schmitt Trigger	HD14584BFP		QQF14584AB
M34	IC, C-MOS, Binary Counter	TC4020BF or	MX-5364	QQF04020AT
		HD14020BFP		QQF04020BB
M35	IC, Hi-speed C-MOS, Inverter	TC40H004F		QQF40004AT
TRANSFORMERS				
OT1	Transformer, Converter			TCA9RZ0423
OT2	Transformer, Modem, AC 1000V		ATB-0499	TDZ19A002K
RESISTORS				
R1	Resistor, Chip	100 ohm/1/8W/±5%		RJ8APJ101%
R2	Resistor, Chip	100K ohm/1/8W/±5%		RJ8APJ104%
R3	Resistor, Chip	390 ohm/1/8W/±5%		RJ8APJ391%
R4	Resistor, Chip	620 ohm/1/8W/±5%	ND-0181EBB	RJ8APJ621%
R5	Resistor, Chip	3.3K ohm/1/8W/±5%		RJ8APJ332%
R6	Resistor, Chip	12K ohm/1/8W/±5%	ND-0288EBB	RJ8APJ123%
R7	Resistor, Chip	620 ohm/1/8W/±5%	ND-0181EBB	RJ8APJ621%
R8	Resistor, Chip	2.2K ohm/1/8W/±5%		RJ8APJ222%
R9	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R10	Resistor, Chip	1K ohm/1/8W/±5%		RJ8APJ102%
R11	Resistor, Chip	68K ohm/1/8W/±5%		RJ8APJ683%
R12	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R13	Resistor, Chip	150K ohm/1/8W/±5%	ND-0384EBB	RJ8APJ154%
R14	Not used			
R15	Resistor, Chip	1K ohm/1/8W/±5%		RJ8APJ102%
R16	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R17	Not used			
R18	Not used			
R19	Resistor, Metal Film	73.2K ohm/1/4W/±1%		RQBPF7322X
R20	Resistor, Metal Film	590K ohm/1/4W/±1%		RQBPF5903X
R21	Resistor, Chip	470K ohm/1/8W/±5%		RJ8APJ474%
R22	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R23	Resistor, Chip	470K ohm/1/8W/±5%		RJ8APJ474%
R24	Resistor, Chip	15K ohm/1/8W/±5%	ND-0297EBB	RJ8APJ153%
R25	Resistor, Metal Film	33.2K ohm/1/4W/±1%		RQBPF3322X
R26	Resistor, Metal Film	52.3K ohm/1/4W/±1%		RQBPF5232X
R27	Resistor, Metal Film	280 ohm/1/4W/±1%	N-01568EE	RQBPF2803X
R28	Resistor, Carbon	10K ohm/1/4W/±5%		RD25PJ103X
R29	Resistor, Carbon	2.2K ohm/1/4W/±5%		RD25PJ222X
R30	Resistor, Metal Film	422K ohm/1/4W/±1%		RQBPF4223X
R31	Not used			
R32	Resistor, Chip	1.8K ohm/1/8W/±5%	ND-00210EBB	RJ8APJ182%
R33	Resistor, Metal Film	3.3K ohm/1/4W/±1%		RQBPF3301X
R34	Resistor, Metal Film	1.3K ohm/1/4W/±1%		RQBPF1301X
R35	Resistor, Metal Film	2.05K ohm/1/4W/±1%		RQBPF2051X
R36	Resistor, Metal Film	806 ohm/1/4W/±1%		RQBPF8060X
R37	Resistor, Metal Film	1.5K ohm/1/4W/±1%		RQBPF1501X

Ref. No.	Description		RS Part No.	Mfr's Part No.
R38	Resistor, Metal Film	665 ohm/1/4W/±1%		RQBPF6650X
R39~R43	Not used			
R44	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R45	Not used			
R46	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R47	Not used			
R48	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R49~R57	Not used			
R58	Resistor, Chip	1.8K ohm/1/8W/±5%	ND-0210EBB	RJ8APJ182%
R59	Resistor, Chip	470K ohm/1/8W/±5%		RJ8APJ474%
R60	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R61	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R62	Resistor, Chip	22K ohm/1/8W/±5%		RJ8APJ223%
R63	Resistor, Chip	750K ohm/1/8W/±5%	ND-0439EBB	RJ8APJ754%
R64	Resistor, Chip	56K ohm/1/8W/±5%		RJ8APJ563%
R65	Resistor, Chip	22K ohm/1/8W/±5%		RJ8APJ223%
R66	Resistor, Chip	1M ohm/1/8W/±5%		RJ8APJ105%
R67	Resistor, Chip	3.3K ohm/1/8W/±5%		RJ8APJ332%
R68	Resistor, Chip	100K ohm/1/8W/±5%		RJ8APJ104%
R69	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R70	Resistor, Chip	200K ohm/1/8W/±5%	ND-0392EBB	RJ8APJ204%
R71	Resistor, Carbon	15M ohm/1/4W/±5%		RD25PJ156X
R72	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R73	Resistor, Chip	68K ohm/1/8W/±5%		RJ8APJ683%
R74	Resistor, Chip	3.3K ohm/1/8W/±5%		RJ8APJ332%
R75	Resistor, Chip	68K ohm/1/8W/±5%		RJ8APJ683%
R76	Resistor, Chip	3.3K ohm/1/8W/±5%		RJ8APJ332%
R77~R80	Not used			
R81	Resistor, Chip	68K ohm/1/8W/±5%		RJ8APJ683%
R82	Resistor, Chip	3.3K ohm/1/8W/±5%		RJ8APJ332%
R83	Not used			
R84	Not used			
R85	Not used			
R86	Resistor, Chip	1M ohm/1/8W/±5%		RJ8APJ105%
R87	Not used			
R88	Resistor, Chip	56K ohm/1/8W/±5%		RJ8APJ563%
R89	Resistor, Chip	1.8K ohm/1/8W/±5%	ND-0210EBB	RJ8APJ182%
R90	Resistor, Chip	47K ohm/1/8W/±5%		RJ8APJ473%
R91	Resistor, Metal Film	150K ohm/1/4W/±1%		RQBPF1503X
R92	Resistor, Metal Film	2.7K ohm/1/4W/±1%		RQBPF2701X
R93	Resistor, Metal Film	94.4K ohm/1/4W/±1%	N-0762BEE	RQBPF9442X
R94	Resistor, Metal Film	22.6K ohm/1/4W/±1%		RQBPF2262X
R95	Resistor, Chip	15K ohm/1/8W/±5%	N-0297EBB	RJ8APJ153%
R96	Resistor, Chip	150K ohm/1/8W/±5%	ND-0384EBB	RJ8APJ154%
R97	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R98	Resistor, Chip	100K ohm/1/8W/±5%		RJ8APJ104%
R99	Resistor, Chip	180K ohm/1/8W/±5%		RJ8APJ184%
R100	Resistor, Chip	1.8K ohm/1/8W/±5%	ND-0210EBB	RJ8APJ182%
R101	Resistor, Chip	150K ohm/1/8W/±5%	ND-0384EBB	RJ8APJ154%
R102	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R103	Resistor, Chip	470 ohm/1/8W/±5%	ND-0169EBB	RJ8APJ471%
R104	Resistor, Chip	470 ohm/1/8W/±5%	ND-0169EBB	RJ8APJ471%
R105	Resistor, Chip	47K ohm/1/8W/±5%		RJ8APJ473%
R106	Resistor, Chip	270 ohm/1/8W/±5%	ND-0155EBB	RJ8APJ271%
R107	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R108	Resistor, Chip	1K ohm/1/8W/±5%		RJ8APJ102%
R109	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R110	Resistor, Chip	22K ohm/1/8W/±5%		RJ8APJ223%
R111	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%

Ref. No.	Description		RS Part No.	Mfr's Part No.
R112	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R113	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R114	Resistor, Chip	100 ohm/1/8W/±5%		RJ8APJ101%
R115	Resistor, Chip	82K ohm/1/8W/±5%		RJ8APJ823%
R116	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R117	Resistor, Chip	1M ohm/1/8W/±5%		RJ8APJ105%
R118	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R119	Resistor, Chip	15K ohm/1/8W/±5%		RJ8APJ153%
R120	Resistor, Chip	15K ohm/1/8W/±5%		RJ8APJ153%
R121	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R122	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R123	Resistor, Chip	10K ohm/1/8W/±5%		RJ8APJ103%
R124	Resistor, Chip	150K ohm/1/8W/±5%	ND-0384EBB	RJ8APJ154%
R125	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R126	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R127	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R128	Resistor, Chip	510K ohm/1/8W/±5%	ND-0428EBB	RJ8APJ514%
R129	Resistor, Chip	510K ohm/1/8W/±5%	ND-0428EBB	RJ8APJ514%
R130	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R131	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R132	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R133	Resistor, Chip	100K ohm/1/8W/±5%		RJ8APJ104%
R134	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R135	Resistor, Chip	510K ohm/1/8W/±5%	ND-0428EBB	RJ8APJ514%
R136	Resistor, Chip	100 ohm/1/8W/±5%		RJ8APJ101%
R137	Resistor, Chip	150K ohm/1/8W/±5%		RJ8APJ154%
R138	Not used			
R139	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R140	Resistor, Chip	1K ohm/1/8W/±5%		RJ8APJ102%
R141 ~ R144	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R145	Resistor, Chip	3.3K ohm/1/8W/±5%		RJ8APJ332%
R146	Not used			
R147 ~ R154	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R155	Resistor, Chip	100K ohm/1/8W/±5%		RJ8APJ104%
R156	Resistor, Chip	100K ohm/1/8W/±5%		RJ8APJ104%
R157	Resistor, Chip	100K ohm/1/8W/±5%		RJ8APJ104%
R158	Resistor, Chip	330 ohm/1/8W/±5%	ND-0159EBB	RJ8APJ331%
R159	Resistor, Chip	330 ohm/1/8W/±5%	ND-0159EBB	RJ8APJ331%
R160	Resistor, Chip	330 ohm/1/8W/±5%	ND-0159EBB	RJ8APJ331%
R161	Resistor, Chip	6.2K ohm/1/8W/±5%	ND-0260EBB	RJ8APJ622%
R162	Resistor, Chip	18K ohm/1/8W/±5%	ND-0303EBB	RJ8APJ183%
R163	Not used			
R164	Resistor, Chip	1.8K ohm/1/8W/±5%	ND-0210EBB	RJ8APJ182%
R165	Resistor, Carbon	27 ohm/1/2W/±5%		RD50TJ270X
R166	Resistor, Chip	4.7K ohm/1/8W/±5%		RJ8APJ472%
R167	Resistor, Chip	33K ohm/1/8W/±5%		RJ8APJ333%
R168	Resistor, Chip	22 ohm/1/8W/±5%		RJ8APJ220%
R169 ~ R193	Resistor, Chip	100K ohm/1/8W/±5%		RJ8APJ104%
R194	Resistor, Chip	1K ohm/1/8W/±5%		RJ8APJ102%
R195	Resistor, Chip	1K ohm/1/8W/±5%		RJ8APJ102%
R196	Resistor, Chip	6.2K ohm/1/8W/±5%	ND-0260EBB	RJ8APJ622%
R197	Resistor, Chip	18K ohm/1/8W/±5%	ND-0303EBB	RJ8APJ183%
R198	Resistor, Chip	6.2K ohm/1/8W/±5%	ND-0260EBB	RJ8APJ622%

Ref. No.	Description	RS Part No.	Mfr's Part No.
R199	Resistor, Chip 18K ohm/1/8W/±5%	ND-0303EBB	RJ8APJ183%
R200 ~ R211	Resistor, Chip 100K ohm/1/8W/±5%		RJ8APJ104%
R212	Resistor, Chip 56K ohm/1/8W/±5%		RJ8APJ563%
R213	Resistor, Chip 47 ohm/1/8W/±5%		RJ8APJ470%
R214	Resistor, Chip 1.2K ohm/1/8W/±5%		RJ8APJ122%
R215	Resistor, Chip 150K ohm/1/8W/±5%	ND-0384EBB	RJ8APJ154%
R216	Resistor, Chip 100 ohm/1/8W/±5%		RJ8APJ101%
R218	Resistor, Metal Oxide 33 ohm/1/2W/±5%		RGHASJ330B
RESISTOR ARRAYS			
RA1	Resistor Array 100K ohm x 8/1/8W/±20%		RAB104M08X
RA2	Resistor Array 33K ohm x 4/1/8W/±20%	ARX-0419	RAB333M04X
RA3	Resistor Array 100K ohm x 4/1/8W/±20%	ARX-0418	RAB104M04N
RELAYS			
RY1	Relay FBR21D05-P	AR-8167	ZRA266001Z
RY2	Relay RY-5W	AR-8168	ZRA266101Z
RY3	Relay FRL-764D05/1AS-T		ZRA164102Z
SWITCHES			
SW1	Switch, Push, SPJ312U, without RESET Knob		SP01ABA06A
SW2	Switch, Slide, Shorting, with Knob - MODEM		SS020259ZA
TRANSISTORS			
T1	Transistor, Silicon, 2SC2712, NPN, NO-Rank	MX-6472	QUC2712XEP
T2	Transistor, Silicon, 2SC2712, NPN, NO-Rank	MX-6472	QUC2712XEP
T3	Transistor, Silicon, 2SC2712, NPN, NO-Rank	MX-6472	QUC2712XEP
T4~T10	Not used		
T11	Transistor, Silicon, 2SC2712, NPN, NO-Rank	MX-6472	QUC2712XEP
T12	Transistor, Silicon, 2SC2712, NPN, NO-Rank	MX-6472	QUC2712XEP
T13	Not used		
T14	Not used		
T15	Transistor, Silicon, 2SC2712, NPN, NO-Rank	MX-6472	QUC2712XEP
T16	Transistor, Silicon, 2SC2712, NPN, Y-Rank	MX-6470	QUC2712XBP
T17	Transistor, Silicon, 2SC2712, NPN, Y-Rank	MX-6470	QUC2712XBP
T18	Transistor, Silicon, 2SC3052, NPN, NO-Rank		QUC3052XAE
T19	Transistor, Silicon, 2SC3052, NPN, NO-Rank		QUC3052XAE
T20	Transistor, Silicon, 2SD1051, NPN, Q-Rank	2SD-1051	QTD1051XAN
T21	Transistor, Silicon, 2SC2712, NPN, GR-Rank	MX-6471	QUC2712XCP
T22	Transistor, Silicon, 2SC2712, NPN, NO-Rank	MX-6472	QUC2712XEP
T23	Transistor, Silicon, 2SA1162, PNP, YG-Rank	MX-6469	QUA1162XDP
T24	Transistor, Silicon, 2SA1162, PNP, YG-Rank	MX-6469	QUA1162XDP
T25~T30	Transistor, Silicon, 2SC2712, NPN, NO-Rank	MX-6472	QUC2712XEP
T31	Transistor, Silicon, 2SA1162, PNP, YG-Rank	MX-6469	QUA1162XDP
T32	Transistor, Silicon, 2SC2712, NPN, NO-Rank	MX-6472	QUC2712XEP
T33	Transistor, Silicon, 2SA1162, PNP, YG-Rank	MX-6469	QUA1162XDP
T34	Transistor, Silicon, 2SA1162, PNP, YG-Rank	MX-6469	QUA1162XDP
THERMISTORS			
TH1	Thermistor 10K ohm ±5%		QHQ5C31HZP
TH2	Thermistor 10K ohm ±5%		QHQ5C31HZP
TH3	Thermistor 10K ohm ±5%		QHQ5C31HZP

Ref. No.	Description	RS Part No.	Mfr's Part No.
VARIABLE RESISTORS			
VR1	Variable Resistor, Semi-fixed, 50K B-Curve - Modem		RPSNB50303
VR2	Variable Resistor, 50K B-Curve - LCD CONTRAST	P-7424	RPSNB50306
CRYSTAL OSCILLATORS			
X1	Crystal Oscillator HC43/U, 1MHz		XAZ1C2001X
X2	Crystal Oscillator 3.579545MHz	ACA-8376	XAZ1B6001X
X3	Crystal Oscillator 4.9152MHz		XBR1A1003X
ZENER DIODE			
ZD1	Diode, Zener, Silicon, RD4.3 EL3		QDZ4R3EL3A
SURGE ABSORBERS			
ZNR1	Surge Absorber ERZ-C10K220, 250A		QNDDK220AN
ZNR2	Surge Absorber ERZ-C10DK361		QNHDK361AN
ZNR3	Surge Absorber SNR-7D18L		QNB7D18LAD

LCD PCB Assembly

Ref. No.	Description		RS Part No.	Mfr's Part No.
CAPACITORS				
C501 ~ C508	Capacitor, Ceramic	0.1μF/25V/+80 -20%		CFKC104ZF%
C509	Not used			
C510	Not used			
C511 ~ C529	Capacitor, Ceramic	0.1μF/25V/+80 -20%		CFKC104ZF%
CONNECTOR				
CN501	Jack, Junction from Main PCB		AJ-7623	YJF10S065Z
INTEGRATED CIRCUITS				
M501 ~ M506	IC, Hi-speed C-MOS, Driver	HD61100	MX-6477	QQF61100AB
M507	IC, Hi-speed C-MOS, Driver	HD61103	MX-6478	QQF61103AB
M508	IC, Hi-speed C-MOS, Driver	HD61103	MX-6478	QQF61103AB
M509	IC, Hi-speed C-MOS, Op-Amp.	LA6324M	MX-6476	QQF06324AC
M510	IC, Hi-speed C-MOS, Counter	TC40H390		QQF40390AT
M511	IC, Hi-speed C-MOS, OR Gate	TC40H386		QQF40386AT
RESISTORS				
R501	Resistor, Chip	1K ohm/1/8W/±2%	ND-0196CBB	RJ8AMG102%
R502	Resistor, Chip	1K ohm/1/8W/±2%	ND-0196CBB	RJ8AMG102%
R503	Resistor, Chip	10K ohm/1/8W/±2%		RJ8AMG103%
R504	Resistor, Chip	1K ohm/1/8W/±2%	ND-0196CBB	RJ8AMG102%
R505	Resistor, Chip	1K ohm/1/8W/±2%	ND-0196CBB	RJ8AMG102%
R506 ~ R509	Resistor, Chip	10K ohm/1/8W/±5%		RJ8AMJ103%
R510 ~ R515	Resistor, Chip	15 ohm/1/8W/±5%	ND-0074EBB	RJ8AMJ150%
R516	Resistor, Chip	10K ohm/1/8W/±2%		RJ8AMG103%

Memory PCB Assembly

Ref. No.	Description		RS Part No.	Mfr's Part No.
CAPACITORS				
C301	Capacitor, Ceramic	0.022μF/16V/±30%	CC-223NDCA	CKV1223N2Y
C302	Not used			
C303	Not used			
C304	Capacitor, Ceramic	0.022μF/16V/±30%	CC-223NDCA	CKV1223N2Y
C305	Capacitor, Ceramic	0.022μF/16V/±30%	CC-223NDCA	CKV1223N2Y
C306	Capacitor, Ceramic	30pF/50V/±10%		CCGB300KON
C307	Capacitor, Ceramic	30pF/50V/±10%		CCGB300KON
C308	Not used			
C309	Not used			
C310	Not used			
C311	Capacitor, Tantalum	1μF/10V/±20%		CSPC010MLN
C312	Capacitor, Tantalum	1μF/10V/±20%		CSPC010MLN
C313	Capacitor, Tantalum	1μF/10V/±20%		CSPC010MLN
CONNECTORS				
CN301	Jack, Junction from Main PCB		AJ-7633	YJF40S012Z
CN302	Jack, Junction from Main PCB		AJ-7635	YJF04S071Z
DIODE				
D301	Diode, Silicon 1S2076			QDSS2076#B
INTEGRATED CIRCUITS				
M301	IC, C-MOS, Timer	RP5C01	MX-6486	QQ005C01AZ
M302	IC, Hi-speed C-MOS, Decoder	TC40H138F		QQ040138AT
M303	IC, C-MOS, RAM	HM6264LP-15	MX-6473	QQ006264AB
M304	IC, C-MOS, RAM	HM6264LP-15	MX-6473	QQ006264AB
M305	IC, C-MOS, RAM	HM6264LP-15	MX-6473	QQ006264AB
RESISTOR				
R301	Resistor, Carbon	100K ohm/1/4W/±5%		RD25PJ104X
SWITCH				
SW302	Switch, Slide, SLD-22B9-03, BACK-UP			SS020260ZL
CRYSTAL OSCILLATOR				
X301	Crystal Oscillator, 32.768kHz ±20ppm			XTR1A1001%

Keyboard Assembly

Ref. No.	Description	RS Part No.	Mfr's Part No.
1-1	Keytop Kit		AGX1000*01
1-1-1	Keytop - TACT		VK121SB007
1-1-2	Keytop - 1		VK122SB004
1-1-3	Keytop - 2		VK122SB005
1-1-4	Keytop - 3		VK122SB006
1-1-5	Keytop - 4		VK122SB007
1-1-6	Keytop - 5		VK122SB008
1-1-7	Keytop - 6		VK122SB009
1-1-8	Keytop - 7		VK122SB010
1-1-9	Keytop - 8		VK122SB011
1-1-10	Keytop - 9		VK122SB012
1-1-11	Keytop - 0		VK122SB013
1-1-12	Keytop - A		VK122SB014
1-1-13	Keytop - B		VK122SB015
1-1-14	Keytop - C		VK122SB016
1-1-15	Keytop - D		VK122SB017
1-1-16	Keytop - E		VK122SB018
1-1-17	Keytop - F		VK122SB019
1-1-18	Keytop - G		VK122SB020
1-1-19	Keytop - H		VK122SB021
1-1-20	Keytop - I		VK122SB022
1-1-21	Keytop - J		VK122SB023
1-1-22	Keytop - G		VK122SB024
1-1-23	Keytop - L		VK122SB025
1-1-24	Keytop - M		VK122SB026
1-1-25	Keytop - N		VK122SB027
1-1-26	Keytop - O		VK122SB028
1-1-27	Keytop - P		VK122SB029
1-1-28	Keytop - Q		VK122SB030
1-1-29	Keytop - R		VK122SB031
1-1-30	Keytop - S		VK122SB032
1-1-31	Keytop - T		VK122SB033
1-1-32	Keytop - U		VK122SB034
1-1-33	Keytop - V		VK122SB035
1-1-34	Keytop - W		VK122SB036
1-1-35	Keytop - X		VK122SB037
1-1-36	Keytop - Y		VK122SB038
1-1-37	Keytop - Z		VK122SB039
1-1-38	Keytop - ESC		VK122SB040
1-1-39	Keytop - MINUS		VK122SB041
1-1-40	Keytop - PLUS		VK122SB042
1-1-41	Keytop - DEL		VK122SB043
1-1-42	Keytop - BRACKET		VK122SB044
1-1-43	Keytop - ;		VK122SB045
1-1-44	Keytop - QUOTATION		VK122SB046
1-1-45	Keytop - CAPSL		VK122SB047
1-1-46	Keytop - COMMA		VK122SB048
1-1-47	Keytop - PERIOD		VK122SB049
1-1-48	Keytop - /		VK122SB050
1-1-49	Keytop - GRPH		VK122SB051
1-1-50	Keytop - CODE		VK122SB052
1-1-51	Keytop - NUM		VK122SB053
1-1-52	Keytop - CURSOR (LEFT-RIGHT)	AK-5652	VK122SB141
1-1-53	Keytop - CURSOR (UP-DOWN)	AK-5653	VK122SB142
1-1-54	Keytop - TAB		VK132SB006
1-1-55	Keytop - CTRL		VK132SB007
1-1-56	Keytop - SHIFT	AK-5654	AV132SB008
1-1-57	Keytop - ENTER	AK-5655	VK142SB003
1-1-58	Keytop - SPACE		VK172SB002

Ref. No.	Description	RS Part No.	Mfr's Part No.
1-2	Keyboard Kit		AGX1000*02
1-2-1	Sprint - SPACE Key	ARB-7737	MW261LJ019
1-2-2	Guide - ENTER Key	AHC-3111	MX422LJ003
1-2-3	Guide - SPACE Key	AHC-3112	MX722LJ002
1-2-4	Lever Guide - ENTER and SPACE Key	AHC-3113	VK112SB001
1-2-5	Lever Stopper - ENTER and SPACE Key	AHC-3114	VK113SH001
1-2-6	Key Guide Pin - SPACE Key	AHC-3115	VM253SH001
1-2-7	Key Guide - SPACE Key	AHC-3116	VM276SB001
1-3	Diode, Silicon 1S2076		QDSS2076#B
1-4	Switch, Key - Tact	AS-2910	SK0101X22T
1-5	Switch, Key - Lock		SK0111X08A
1-6	Switch, Key - Push	AS-2911	SK0111X12A
1-7	Knob, Switch, Black, POWER	AK-5656	VB111SB002
1-8	Support, Keyboard	AHC-3117	VM266NW001
1-9	Insulator		VS873YB001
CN401	Jack, Junction from Main PCB	AJ-7622	YJF22S014Z
LED401	LED, SLP-135B		QL1SP135BC
PSW401	Switch, Push, POWER ON/OFF	AS-2912	SP01ABX56A

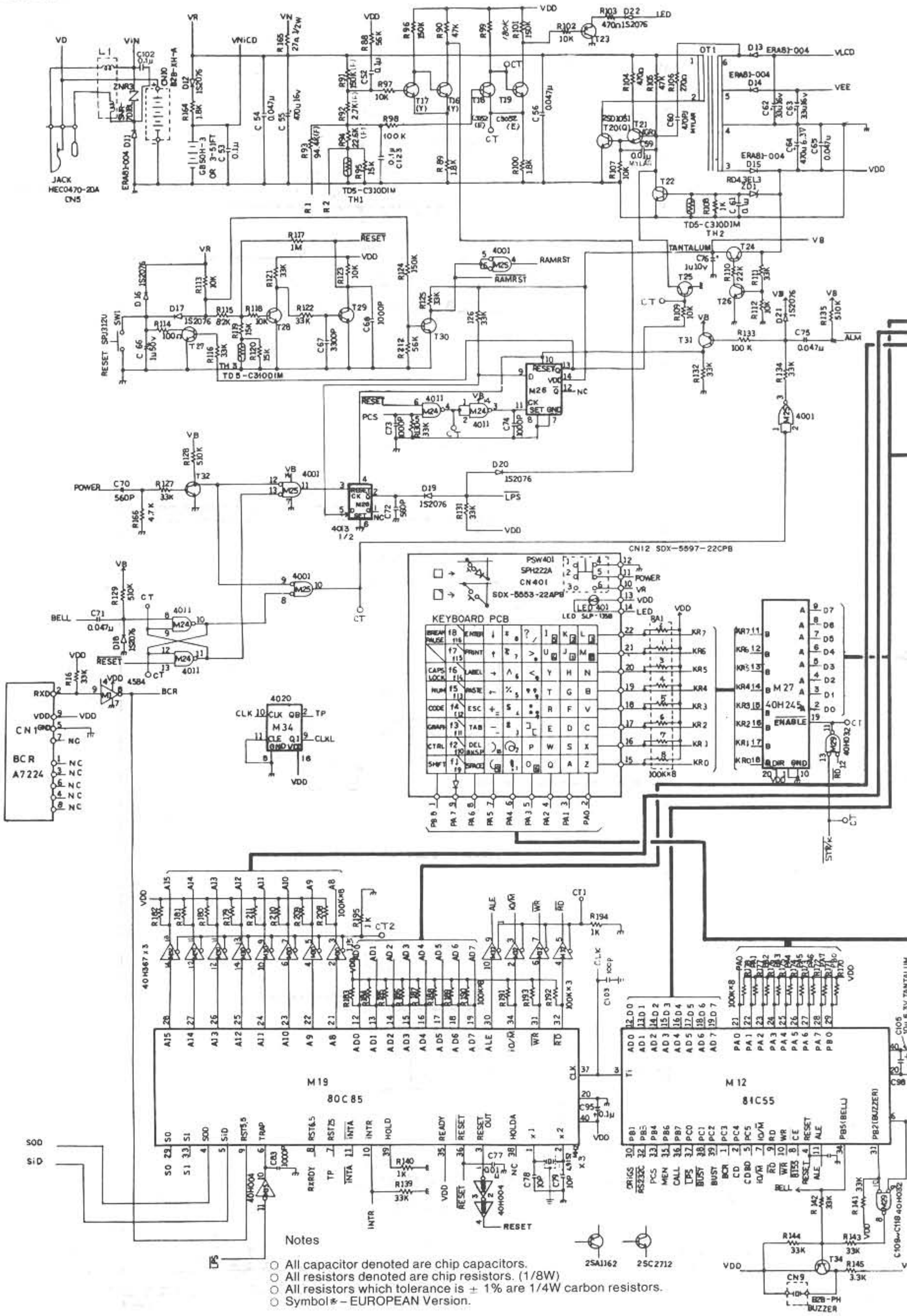
Mechanical and Assembly Parts

Ref. No.	Description	RS Part No.	Mfr's Part No.
1	Keyboard Assembly	AXX-0230	AFLX1000*1
2	LCD PCB Assembly	AX-9503	APLX140BBC
2-1	Frame, LCD		MB871SZ013
2-2	Connector, LCD to Dummy	AJ-7624	VQ711RW002
2-3	Connector, LCD to Segment	AJ-7625	VQ811RC001
2-4	Connector, LCD to Common	AJ-7626	VU711RC001
2-5	LCD, LR217-C	AL-1485	ZXLR217CXB
3	Main PCB Assembly	AX-9504	APLX141ABC
3-1	Knob, CONTRAST, Black	AK-5657	VF187SB003
3-2	Knob, RESET, Black		VK121SB004
3-3	Socket, IC, DICF-28CS		YSC28S005Z
3-4	Battery, Nickel-Cadmium, 3-51FT		ZBN036102Y
3-5	Buzzer Assembly	AB-7129	AYX1000*01
3-6	Nut, M2.6, S-ZNCR, Thin Type	AHD-7322	BNHCL26NSZ
3-7	Screw, Pan Head, CEMS, Machine, M3 x 8, S-ZNCR	AHD-2926	BSPC3008NZ
3-8	Screw, Pan Head, Machine, M2.6 x 12, S-ZNCR	AHD-2927	BSPP2612NZ
3-9	Screw, Pan Head, Machine, M1.7 x 3, S-Black		BSP21703NB
4	Memory PCB Assembly	AX-9505	APLX150ABZ
4-1	Socket, IC, ICC05-028-360TP-2		YSC28S006Z
4-2	Socket, IC, 5500-28A	AJ-7637	YSC28S007Z
5	Connector and Cord, to Battery	AW-3267	ACCNM07GEA
6	Case Assembly, Top, Ivory	AZ-7166	AMX1000*01
6-1	Retainer, LCD	AHC-3118	MF111SM001
6-2	Cover, Protector for Main PCB	ART-5550	VB553SW001
6-3	Case, Top, Ivory		VB884SW002
6-4	Plate, Model		VVMX1000*2
7	Case Assembly, Bottom, Black	AZ-7167	AMX1000*02
7-1	Terminal, Battery, Plus and Minus	AB-0616	MW261LJ020
7-2	Case, Bottom, Black		VB882SB001
7-3	Foot, Rubber	AF-1258	VS708RH001
8	LCD Case Assembly, Bottom, Ivory	AZ-7168	AMX1000*04
8-1	Case, Bottom, LCD, Ivory		VB872SW015
8-2	Filter		VS878AC001
8-3	Plate, Magnet		MS607FJ001
8-4	Magnet, Box		MM111SN002
8-5	Pad, Magnet		VF822SB001
9	Screw, Bind Head with Outside Toothed Washer, Machine, M3 x 6, S-ZNCR	AHD-2928	BSP#3006NZ
10	Screw, Bind Head, Machine, M3 x 8, S-ZNCR	AHD-2929	BTPP3008PZ
11	Plate, Name	AHC-3119	KLX1****01
12	Label, FCC (USA Version only)		KL000394XX
14	Plate, Serial Number (For USA Version)		KL000525XX
	(For CANADA Version)		MVSX1000*2
15	Terminal, Battery, Minus	AB-0617	MW161SN003
16	Terminal, Battery, Plus	AB-0618	MS218SN001
17	Cover, Inner		VB553SW001
18	Cap, System Bus Connector Cover	ART-5553	VB611SB001
19	Shaft, Support-Right	ART-5554	VB632SW007
20	Shaft, Support-Left	ART-5555	VB632SW006
21	Cover, Cable, Ivory		VB742SW001
22	Case, Top, LCD, Ivory	AZ-7169	VB872SW014
23	Cap, B.C.R. Connector Cover		VE32JPB001
24	Knob, Switch, Modem	AK-5658	VK121SB006
25	Cover, Battery	ADB-0457	VS758SB001
26	Cover, ROM and RAM	AZ-7170	VS767SB001
27	Shaft, LCD-Left	ART-5557	VT665NW003
28	Shaft, LCD-Right	ART-5558	VT665NW004
29	Cap, Printer Connector Cover	ART-5559	VU521SB001

Ref. No.	Description	RS Part No.	Mfr's Part No.
30	Flat Cable, UL2896, P1.25	AW-3268	WC22075BD1
31	Flat Cable, UL2896, P1.25	AW-3269	WC40029AD1
32	Flat Cable for LCD	AW-3270	WC10070BD1
33	Supporter		MB321SL001
34	Protector for Flat Cable		VS775FB001
35	Ball		MX444SX001
36	Spring		MB221LX001
	Hardware Kit	AHW-2603860	AYX1000*02
	Screw, Bind Head, Machine, M3 x 8, S-ZNCR		BTPP3008PZ

VII. SCHEMATIC DIAGRAMS/ PCB VIEWS

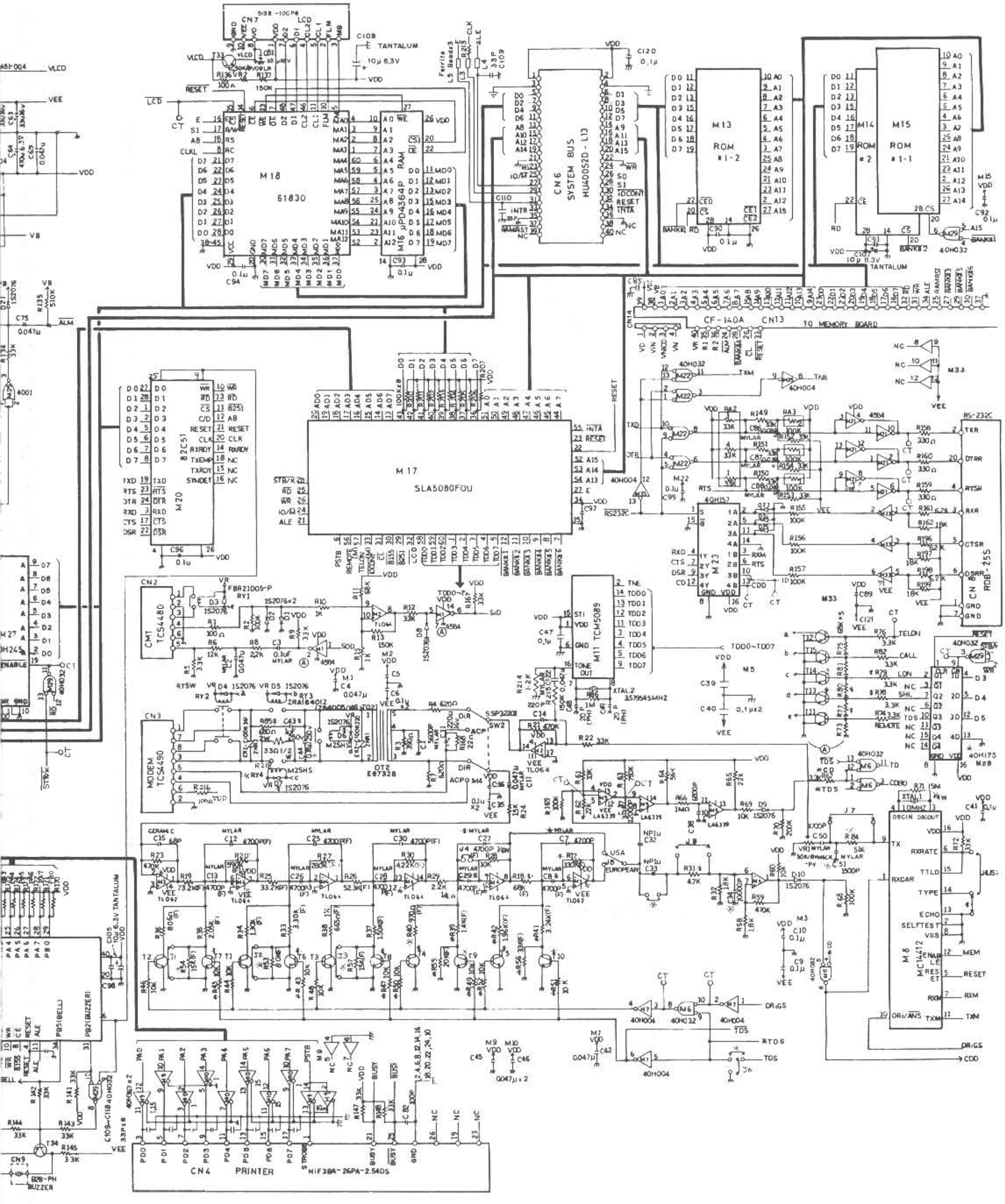
Schematic Diagrams



Notes

- ○ All capacitor denoted are chip capacitors.
- ○ All resistors denoted are chip resistors. (1/8W)
- ○ All resistors which tolerance is ± 1% are 1/4W carbon resistors.
- ○ Symbol* – EUROPEAN Version.

Figure 7-1. Main PC



ure 7-1. Main PCB – Schematic Diagram

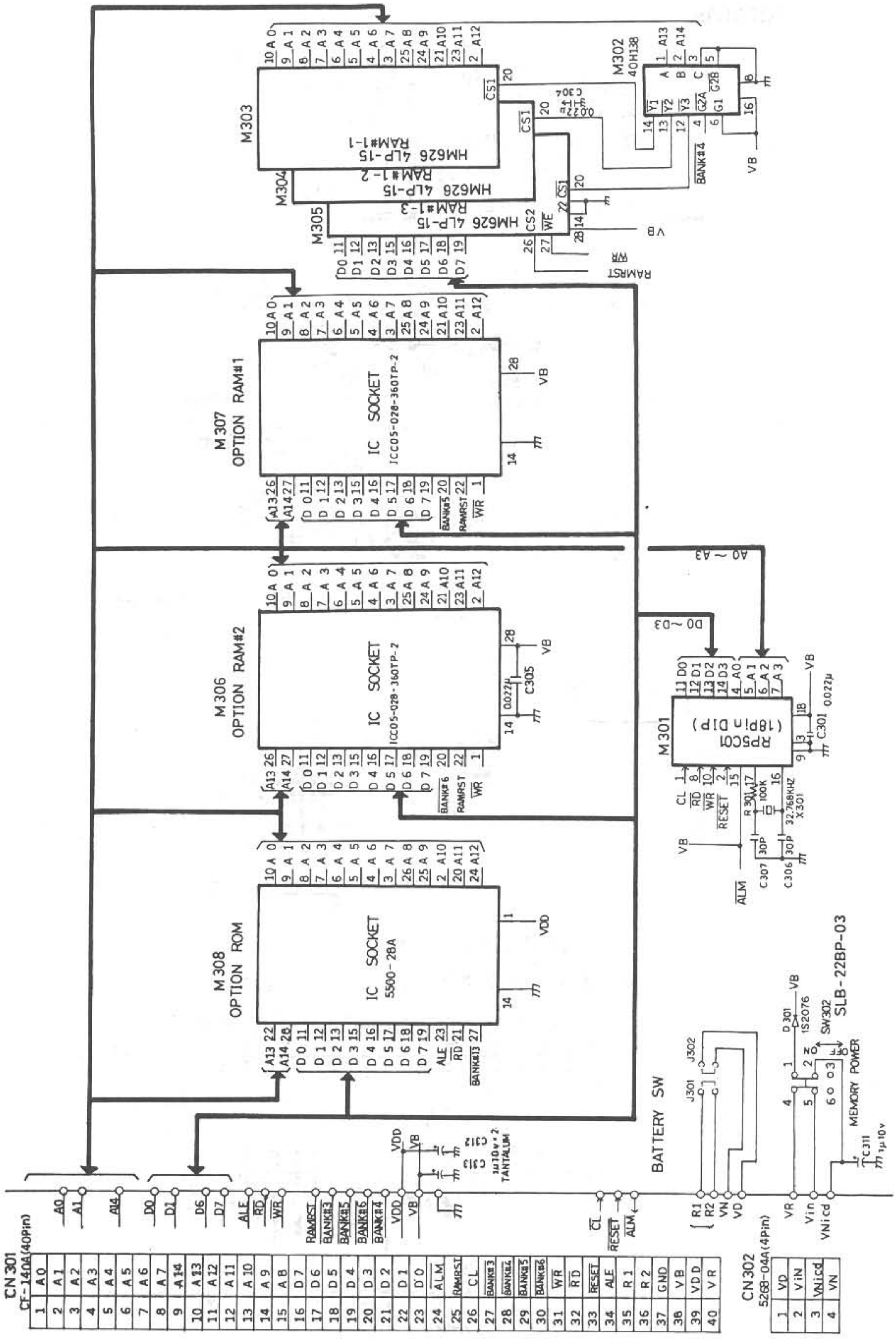


Figure 7-3. Memory PCB – Schematic Diagram

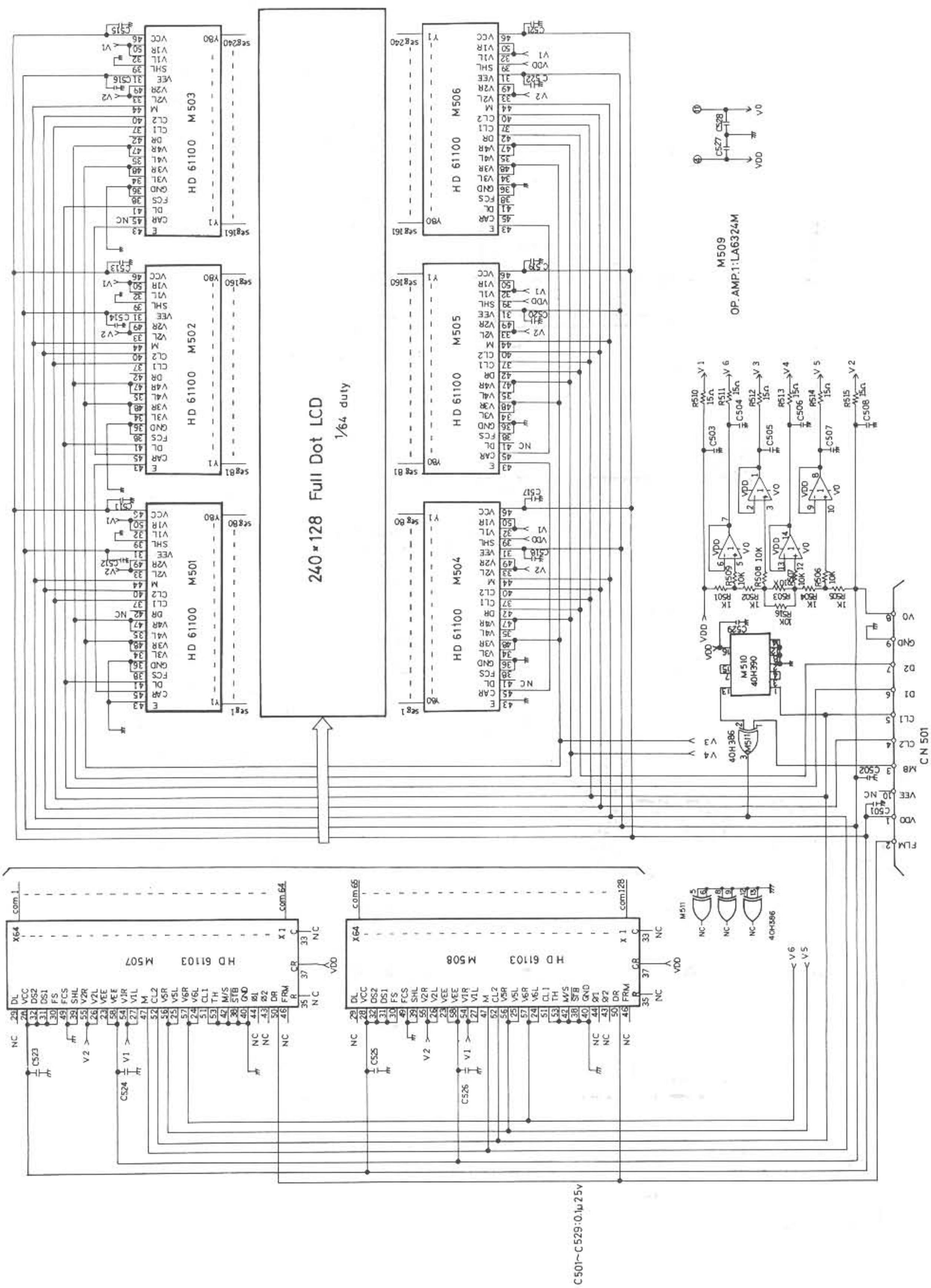


Figure 7-2. LCD PCB – Schematic Diagram

PCB Views

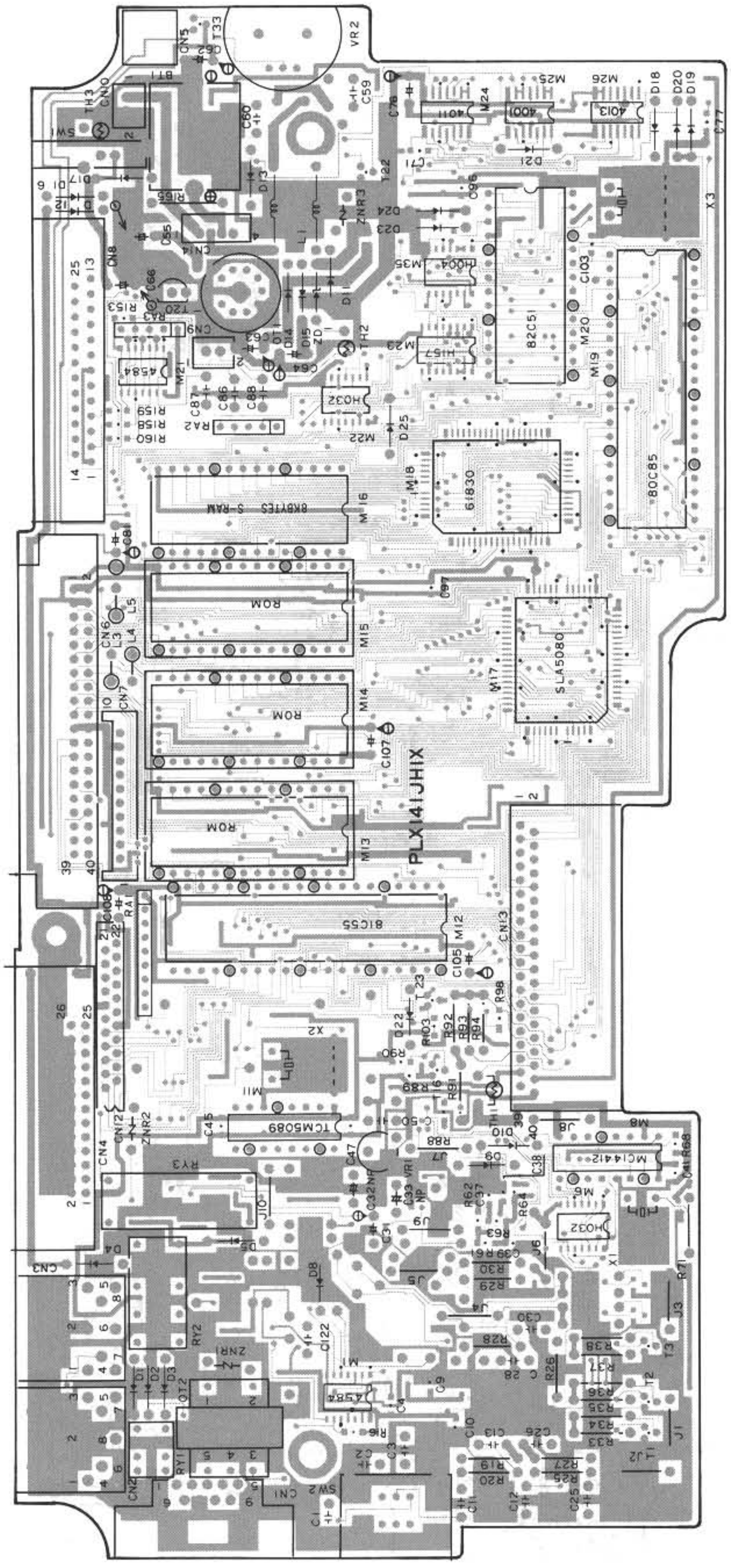


Figure 7-4. Main PCB – Top View

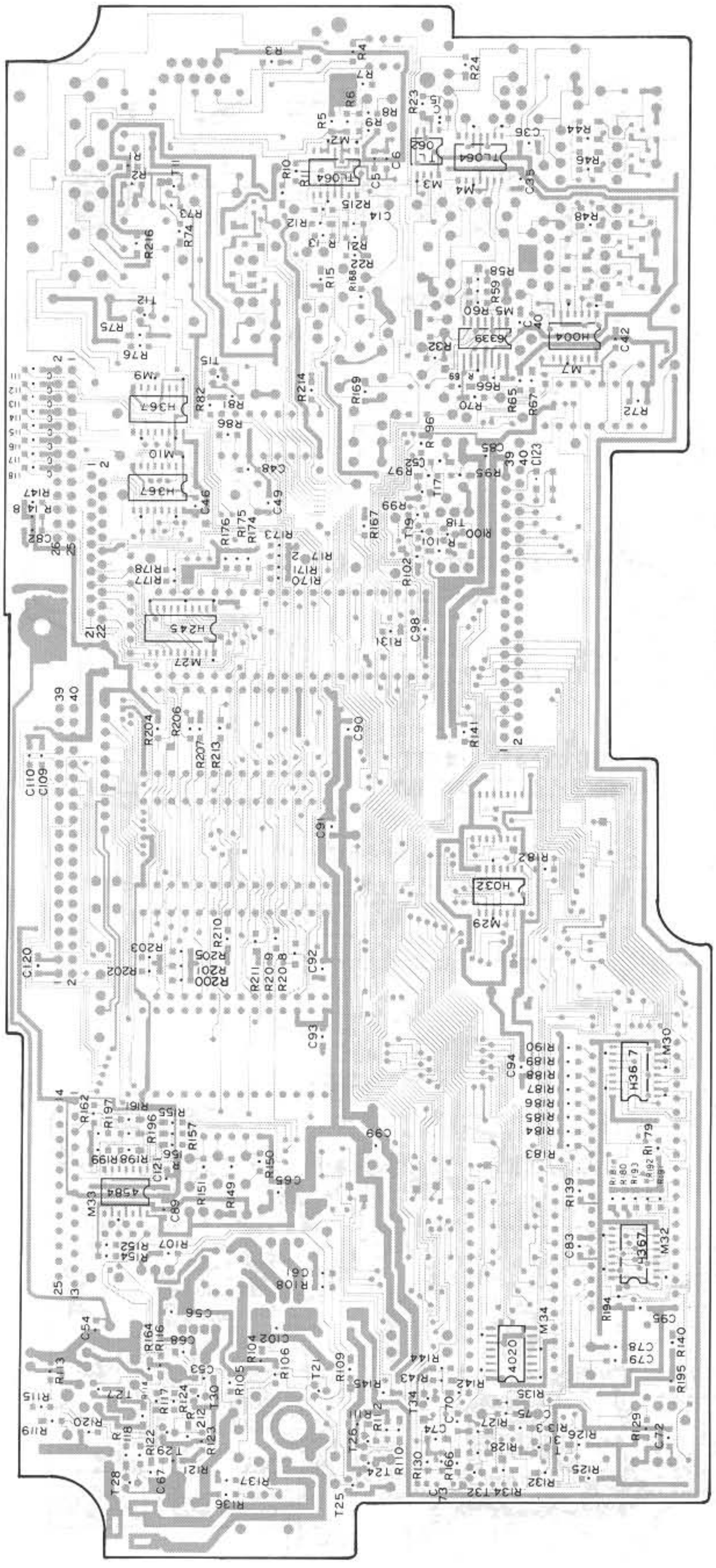


Figure 7-5. Main PCB – Bottom View

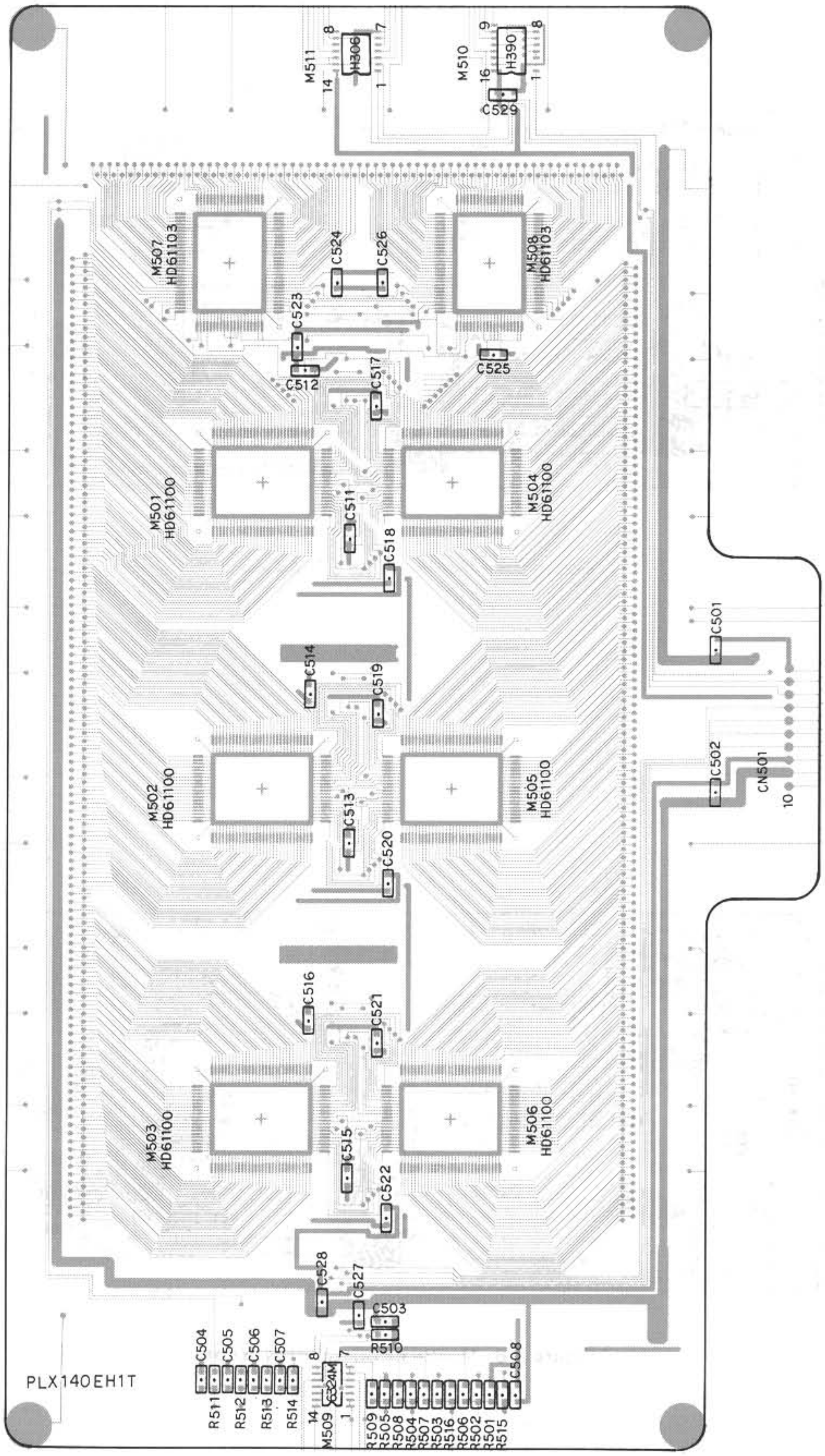


Figure 7-6. LCD PCB – Top View

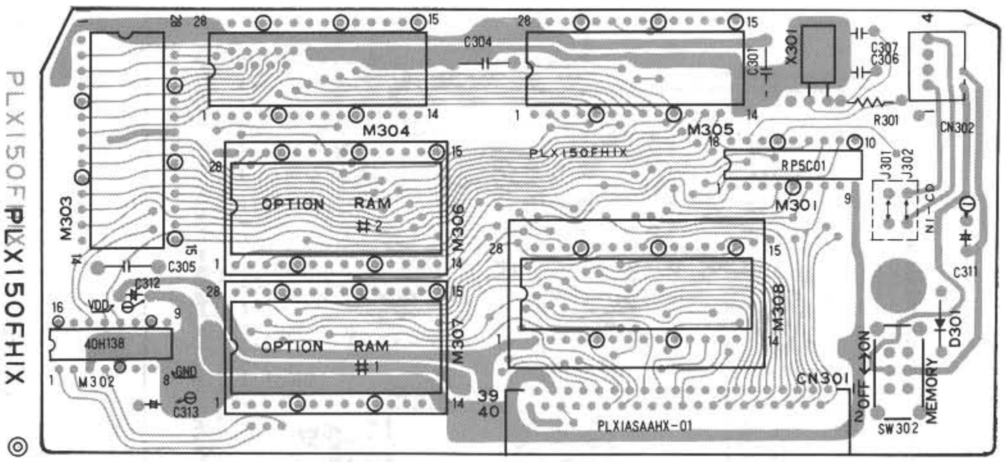


Figure 7-7. Memory PCB – Top View

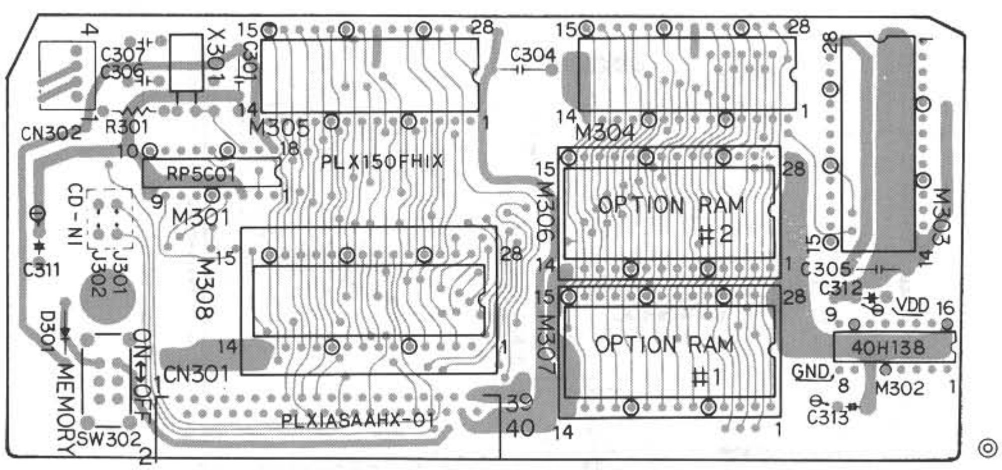


Figure 7-8. Memory PCB – Bottom View

APPENDIX A/INSTALLATIONS

Installation of Optional RAMs and ROM

- Using the coin, remove the optional RAM and ROM cover on the bottom case.
- Insert the optional RAMs into the IC sockets marked M306 and M307.
  In this case, the IC socket M307 is used for the RAM #1 and M306 is RAM #2.
- Insert the optional ROM into the IC socket marked M308.

Installation of Nickel-Cadmium Batteries

- Remove the memory PCB (Refer to Section II, Disassembly Instruction).
- Install the modification jumpers into the through holes marked J301 and J302.
- Re-assemble the unit.

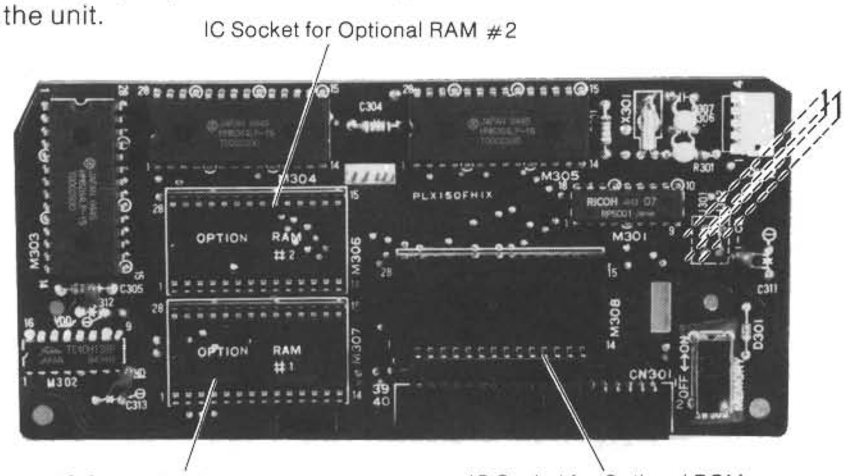


Figure A-1. Memory PCB

- Remove the battery cover and install the four Nickel-Cadmium batteries into the battery compartment.
- Drill the screw hole on the battery cover using the tapping screw Ⓐ and secure the battery cover and bottom case.
- Stick the red label Ⓑ on the battery cover.

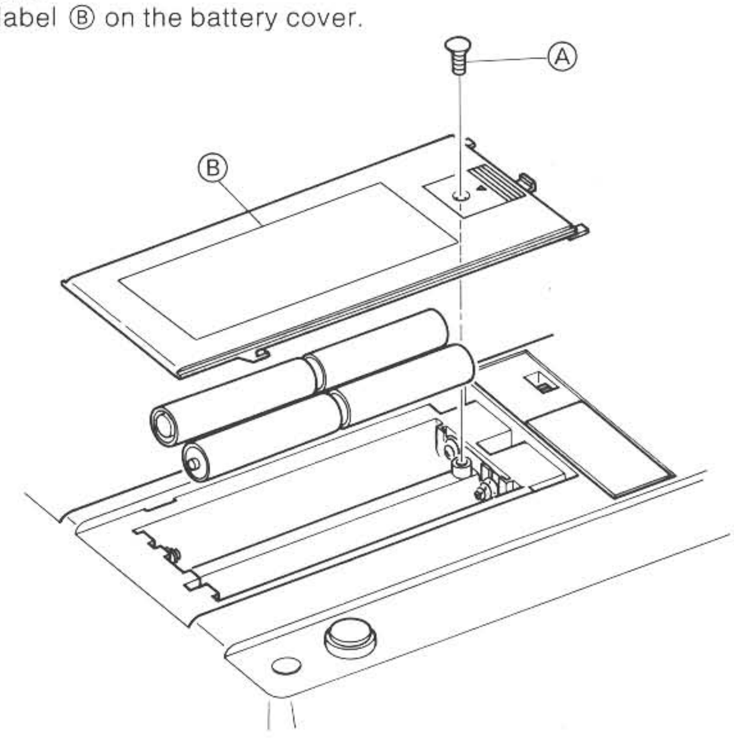


Figure A-2. Installation of Nickel-Cadmium Batteries

APPENDIX B/KEYBOARD LAYOUT, CONNECTOR PIN ASSIGNMENTS AND CHARACTER CODE TABLE

B-1. Keyboard Layout

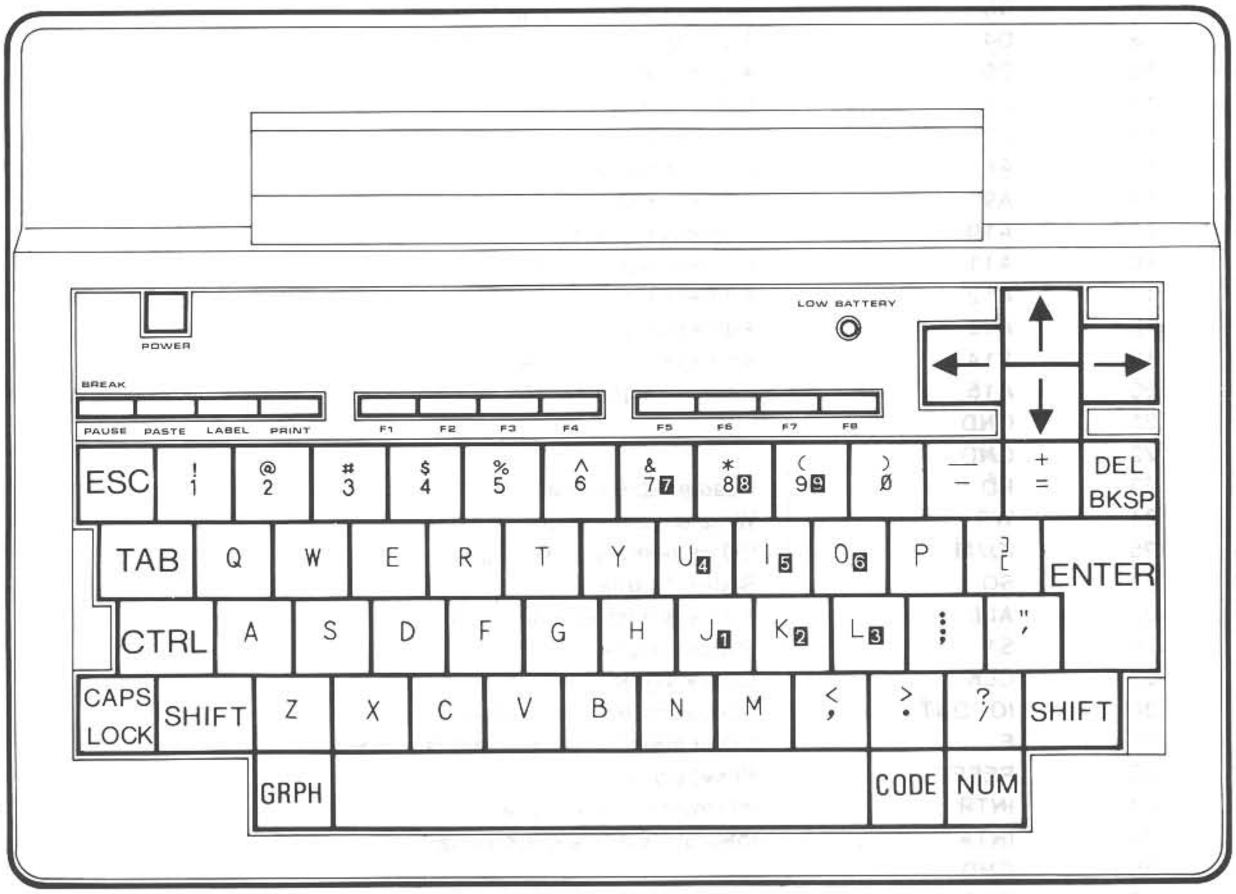


Figure B-1. Keyboard Layout

B-2. Connector Pin Assignments

B-2-1. System Bus Interface

Pin No.	Symbol	Description
1	VDD	
2	VDD	
3	GND	
4	GND	
5	D0	Address and data signal bit 0
6	D1	Address and data signal bit 1
7	D2	Address and data signal bit 2
8	D3	Address and data signal bit 3
9	D4	Address and data signal bit 4
10	D5	Address and data signal bit 5
11	D6	Address and data signal bit 6
12	D7	Address and data signal bit 7
13	A8	Address signal bit 8
14	A9	Address signal bit 9
15	A10	Address signal bit 10
16	A11	Address signal bit 11
17	A12	Address signal bit 12
18	A13	Address signal bit 13
19	A14	Address signal bit 14
20	A15	Address signal bit 15
21	GND	
22	GND	
23	$\overline{RD}$	Read enable signal
24	$\overline{WR}$	Write enable signal
25	IO/$\overline{M}$	I/O or memory select signal
26	SO	Status 0 signal
27	ALE	Address latch enable signal
28	S1	Status 1 signal
29	CLK	CLock signal
30	$\overline{IOCONT}$	I/O controller select signal
31	E	I/O or memory access enable signal
32	RESET	Reset signal
33	$\overline{INTR}$	Interrupt request signal
34	$\overline{INTA}$	Interrupt acknowledge signal
35	GND	
36	GND	
37	$\overline{RAMRST}$	RAM enable signal
38	NC	
39	NC	
40	NC	

Table B-1. System Bus Connector Pin Assignments

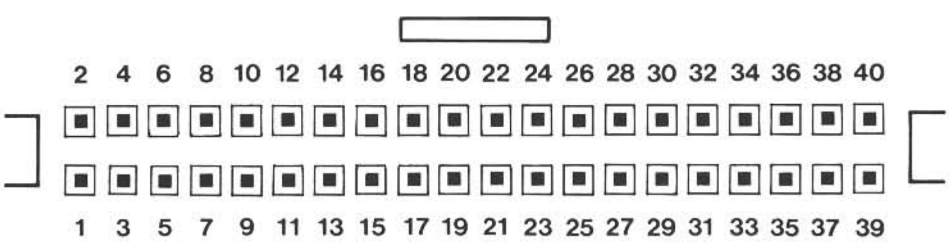


Figure B-2. System Bus Connector

B-2-2. RS-232C Interface

Pin No.	Symbol	Description
1	GND	
2	TXR	Transmit Data
3	RXR	Receive Data
4	RTS	Request to send
5	CTS	Clear to send
6	DSR	Data set ready
7	GND	
8	CD	Carrier detect
9	NC	
10	NC	
11	NC	
12	NC	
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	DTR	Data terminal ready
21	NC	
22	NC	
23	NC	
24	NC	
25	NC	

Table B-2. RS-233C Connector Pin Assignments

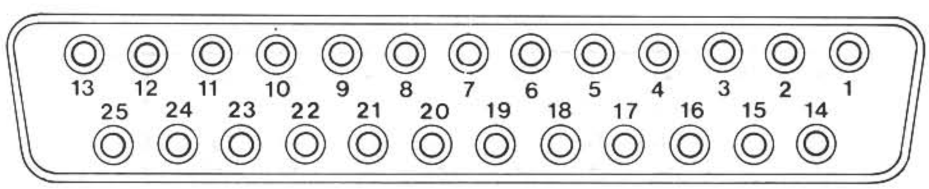


Figure B-3. RS-232C Connector

B-2-3. Printer Interface

Pin No.	Symbol	Description
1	**$\overline{\text{STROBE}}$**	STROBE Pulse
2	**GND**	
3	**PD0**	Bit 0 of Print Data
4	**GND**	
5	**PD1**	Bit 1 of Print Data
6	**GND**	
7	**PD2**	Bit 2 of Print Data
8	**GND**	
9	**PD3**	Bit 3 of Print Data
10	**GND**	
11	**PD4**	Bit 4 of Print Data
12	**GND**	
13	**PD5**	Bit 5 of Print Data
14	**GND**	
15	**PD6**	Bit 6 of Print Data
16	**GND**	
17	**PD7**	Bit 7 of Print Data
18	**GND**	
19	**NC**	
20	**GND**	
21	**BUSY**	Busy signal for Computer
22	**GND**	
23	**NC**	
24	**GND**	
25	**$\overline{\text{BUSY}}$**	Select signal
26	**NC**	

Table B-3. Printer Connector Pin Assignments

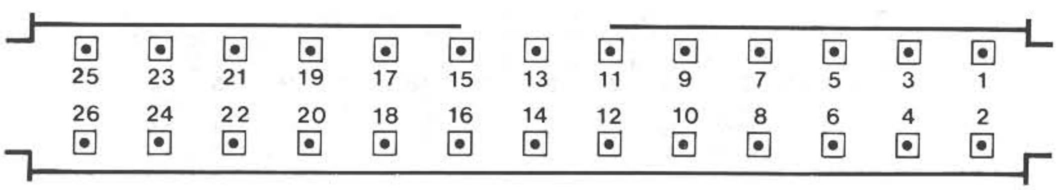


Figure B-4. Printer Connector

B-2-4. Cassette Interface

Pin No.	Symbol	Description
1	**REM 1**	Remote
2	**GND**	
3	**REM 2**	Remote
4	**R × C**	Receive data for CMT
5	**T × C**	Transmit data for CMT
6	**GND**	
7	**NC**	
8	**NC**	

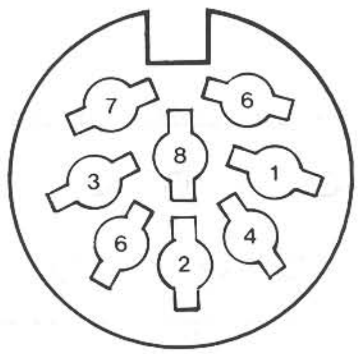


Figure B-5. Cassette Connector

B-2-5. MODEM Interface

Pin No.	Symbol	Description
1	**TL**	Conventional Telephone Unit
2	**GND**	
3	**R × MD**	Direct Connection to Tel Line (RING)
4	**R × MC**	Acoustic Coupler Connection (MIC)
5	**T × MC**	Acoustic Coupler Connection (Speaker)
6	**VDD**	
7	**T × MD**	Direct Connection to Tel Line (TIP)
8	**RP**	Ringing Pulse

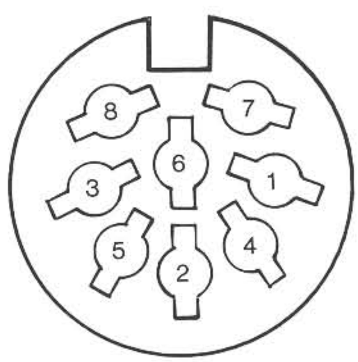


Figure B-6. MODEM Connector

B-2-6. Bar Code Reader Interface

Pin No.	Symbol	Description
1	NC	
2	R x DB	Receive data from bar code reader
3	NC	
4	NC	
5	NC	
6	NC	
7	GND	
8	NC	
9	VDD	

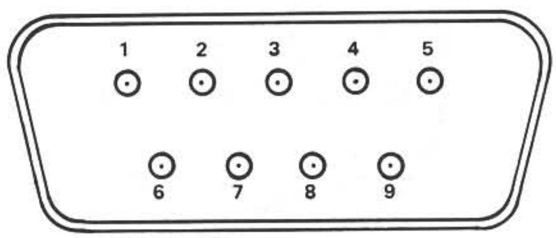


Figure B-7. Bar Code Reader Connector

B-3. Character Code Table

Decimal	Hex	Binary	Displayed Character	Keyboard Character
00	00	00000000		CTRL @
1	01	00000001		CTRL A
2	02	00000010		CTRL B
3	03	00000011		CTRL C
4	04	00000100		CTRL D
5	05	00000101		CTRL E
6	06	00000110		CTRL F
7	07	00000111		CTRL G
8	08	00001000		CTRL H
9	09	00001001		CTRL I
10	0A	00001010		CTRL J
11	0B	00001011		CTRL K
12	0C	00001100		CTRL L
13	0D	00001101		CTRL M
14	0E	00001110		CTRL N
15	0F	00001111		CTRL O
16	10	00010000		CTRL P
17	11	00010001		CTRL Q
18	12	00010010		CTRL R
19	13	00010011		CTRL S
20	14	00010100		CTRL T
21	15	00010101		CTRL U
22	16	00010110		CTRL V
23	17	00010111		CTRL W
24	18	00011000		CTRL X
25	19	00011001		CTRL Y
26	1A	00011010		CTRL Z
27	1B	00011011		ESC
28	1C	00011100		→
29	1D	00011101		←
30	1E	00011110		↑
31	1F	00011111		↓
32	20	00100000		SPACE BAR
33	21	00100001	!	!
34	22	00100010	"	"
35	23	00100011	#	#
36	24	00100100	$	$
37	25	00100101	%	%
38	26	00100110	&	&
39	27	00100111	'	'
40	28	00101000	(	(
41	29	00101001	)	)
42	2A	00101010	*	*
43	2B	00101011	+	+
44	2C	00101100	,	,
45	2D	00101101	–	–
46	2E	00101110	.	.
47	2F	00101111	/	/
48	30	00110000	Ø	0
49	31	00110001	1	1

Decimal	Hex	Binary	Displayed Character	Keyboard Character
50	32	00110010	2	2
51	33	00110011	3	3
52	34	00110100	4	4
53	35	00110101	5	5
54	36	00110110	6	6
55	37	00110111	7	7
56	38	00111000	8	8
57	39	00111001	9	9
58	3A	00111010	:	:
59	3B	00111011	;	;
60	3C	00111100	<	<
61	3D	00111101	=	=
62	3E	00111110	>	>
63	3F	00111111	?	?
64	40	01000000	@	@
65	41	01000001	A	A
66	42	01000010	B	B
67	43	01000011	C	C
68	44	01000100	D	D
69	45	01000101	E	E
70	46	01000110	F	F
71	47	01000111	G	G
72	48	01001000	H	H
73	49	01001001	I	I
74	4A	01001010	J	J

Decimal	Hex	Binary	Display Character	Keyboard Character
75	4B	01001011	K	K
76	4C	01001100	L	L
77	4D	01001101	M	M
78	4E	01001110	N	N
79	4F	01001111	O	O
80	50	01010000	P	P
81	51	01010001	Q	Q
82	52	01010010	R	R
83	53	01010011	S	S
84	54	01010100	T	T
85	55	01010101	U	U
86	56	01010110	V	V
87	57	01010111	W	W
88	58	01011000	X	X
89	59	01011001	Y	Y
90	5A	01011010	Z	Z
91	5B	01011011	[	[
92	5C	01011100	\	GRPH –
93	5D	01011101	]	]
94	5E	01011110	^	
95	5F	01011111	_	_
96	60	01100000	`	GRPH [
97	61	01100001	a	a
98	62	01100010	b	b
99	63	01100011	c	c

Decimal	Hex	Binary	Displayed Character	Keyboard Character
100	64	01100100	d	d
101	65	01100101	e	e
102	66	01100110	f	f
103	67	01100111	g	g
104	68	01101000	h	h
105	69	01101001	i	i
106	6A	01101010	j	j
107	6B	01101011	k	k
108	6C	01101100	l	l
109	6D	01101101	m	m
110	6E	01101110	n	n
111	6F	01101111	o	o
112	70	01110000	p	p
113	71	01110001	q	q
114	72	01110010	r	r
115	73	01110011	s	s
116	74	01110100	t	t
117	75	01110101	u	u
118	76	01110110	v	v
119	77	01110111	w	w
120	78	01111000	x	x
121	79	01111001	y	y
122	7A	01111010	z	z
123	7B	01111011	{	GRPH 9
124	7C	01111100	¦	GRPH _

Decimal	Hex	Binary	Displayed Character	Keyboard Character
125	7D	01111101	}	GRPH 0
126	7E	01111110	~	GRPH]
127	7F	01111111		DEL
128	80	10000000		GRPH p
129	81	10000001		GRPH m
130	82	10000010		GRPH f
131	83	10000011		GRPH x
132	84	10000100		GRPH c
133	85	10000101		GRPH a
134	86	10000110		GRPH h
135	87	10000111		GRPH t
136	88	10001000	π	GRPH 1
137	89	10001001	√	GRPH r
138	8A	10001010	≠	GRPH /
139	8B	10001011	Σ	GRPH s
140	8C	10001100		GRPH '
141	8D	10001101	±	GRPH =
142	BE	10001110	∫	GRPH i
143	BF	10001111		GRPH e
144	90	10010000		GRPH y
145	91	10010001		GRPH u
146	92	10010010		GRPH ;
147	93	10010011		GRPH q
148	94	10010100		GRPH w
149	95	10010101		GRPH b

Decimal	Hex	Binary	Displayed Character	Keyboard Character
150	96	10010110	♀	GRPH n
151	97	10010111	✂	GRPH .
152	98	10011000	↑	GRPH o
153	99	10011001	↓	GRPH ,
154	9A	10011010	→	GRPH l
155	9B	10011011	←	GRPH k
156	9C	10011100	♣	GRPH 2
157	9D	10011101	◇	GRPH 3
158	9E	10011110	♡	GRPH 4
159	9F	10011111	♤	GRPH 5
160	A0	10100000	´	CODE '
161	A1	10100001	à	CODE z
162	A2	10100010	ç	CODE f
163	A3	10100011	£	GRPH 8
164	A4	10100100	`	CODE "
165	A5	10100101	µ	CODE]
166	A6	10100110	◆	CODE)
167	A7	10100111	▼	CODE _
168	A8	10101000	†	CODE +
169	A9	10101001	§	CODE s
170	AA	10101010	®	CODE R
171	AB	10101011	©	CODE Y
172	AC	10101100	¼	CODE p
173	AD	10101101	¾	CODE ;
174	AE	10101110	½	CODE /
175	AF	10101111	¶	CODE 0
176	B0	10110000	¥	GRPH 7
177	B1	10110001	Ä	CODE Q
178	B2	10110010	Ö	CODE O
179	B3	10110011	Ü	CODE U
180	B4	10110100	¢	GRPH 6
181	B5	10110101	~	CODE [
182	B6	10110110	ä	CODE q
183	B7	10110111	ö	CODE o
184	B8	10111000	ü	CODE u
185	B9	10111001	ß	CODE S
186	BA	10111010	™	CODE T
187	BB	10111011	é	CODE d
188	BC	10111100	ù	CODE m
189	BD	10111101	è	CODE c
190	BE	10111110	¨	CODE =
191	BF	10111111	ƒ	CODE F
192	C0	11000000	â	CODE 1
193	C1	11000001	ê	CODE 3
194	C2	11000010	î	CODE 8
195	C3	11000011	ô	CODE 9
196	C4	11000100	û	CODE 7
197	C5	11000101	^	CODE –
198	C6	11000110	ë	CODE e
199	C7	11000111	ï	CODE i

Decimal	Hex	Binary	Displayed Character	Keyboard Character
200	C8	11001000	á	CODE a
201	C9	11001001	í	CODE k
202	CA	11001010	ó	CODE l
203	CB	11001011	ú	CODE j
204	CC	11001100	¡	CODE !
205	CD	11001101	ñ	CODE n
206	CE	11001110	ã	CODE v
207	CF	11001111	õ	CODE b
208	D0	11010000	Æ	CODE X
209	D1	11010001	æ	CODE x
210	D2	11010010	Å	CODE W
211	D3	11010011	å	CODE w
212	D4	11010100	Ø	CODE >
213	D5	11010101	ø	CODE .
214	D6	11010110	Ñ	CODE N
215	D7	11010111	É	CODE D
216	D8	11011000	Á	CODE A
217	D9	11011001	ƒ	CODE K
218	DA	11011010	Ó	CODE L
219	DB	11011011	Ú	CODE J
220	DC	11011100	¿	CODE ?
221	DD	11011101	Ù	CODE M
222	DE	11011110	È	CODE C
223	DF	11011111	À	CODE Z
224	ED	11100000		GRPH Z
225	E1	11100001	▘	GRPH !
226	E2	11100010	▝	GRPH @
227	E3	11100011	▖	GRPH #
228	E4	11100100	▗	GRPH $
229	E5	11100101	▚	GRPH %
230	E6	11100110	▞	GRPH ^
231	E7	11100111	▀	GRPH Q
232	E8	11101000	▄	GRPH W
233	E9	11101001	▌	GRPH E
234	EA	11101010	▐	GRPH R
235	EB	11101011	▛	GRPH A
236	EC	11101100	▜	GRPH S
237	ED	11101101	▙	GRPH D
238	EE	11101110	▟	GRPH F
239	EF	11101111	█	GRPH X
240	F0	11110000	┌	GRPH U
241	F1	11110001	─	GRPH P
242	F2	11110010	┐	GRPH O
243	F3	11110011	┬	GRPH I
244	F4	11110100	├	GRPH J
245	F5	11110101	│	GRPH :
246	F6	11110110	└	GRPH M
247	F7	11110111	┘	GRPH >
248	F8	11111000	┴	GRPH <
249	F9	11111001	┤	GRPH L

Decimal	Hex	Binary	Displayed Character	Keyboard Character
250	FA	11111010	┼	GRPH K
251	FB	11111011	◤	GRPH H
252	FC	11111100	◢	GRPH T
253	FD	11111101	◥	GRPH G
254	FE	11111110	◣	GRPH Y
255	FF	11111111	▒	GRPH C

APPENDIX C/TECHNICAL INFORMATION

C-1. 80C85A

General Description

The 80C85A is a complete 8-bit parallel central processor implemented in silicon gate C-MOS technology and compatible with 8085A.
It is designed with same processing speed and lower power consumption compared with 8085A, thereby offering a high level of system integration.
The 80C85A uses a multiplexed address/data bus. The address is split between the 8-bit address bus and the 8-bit data bus.

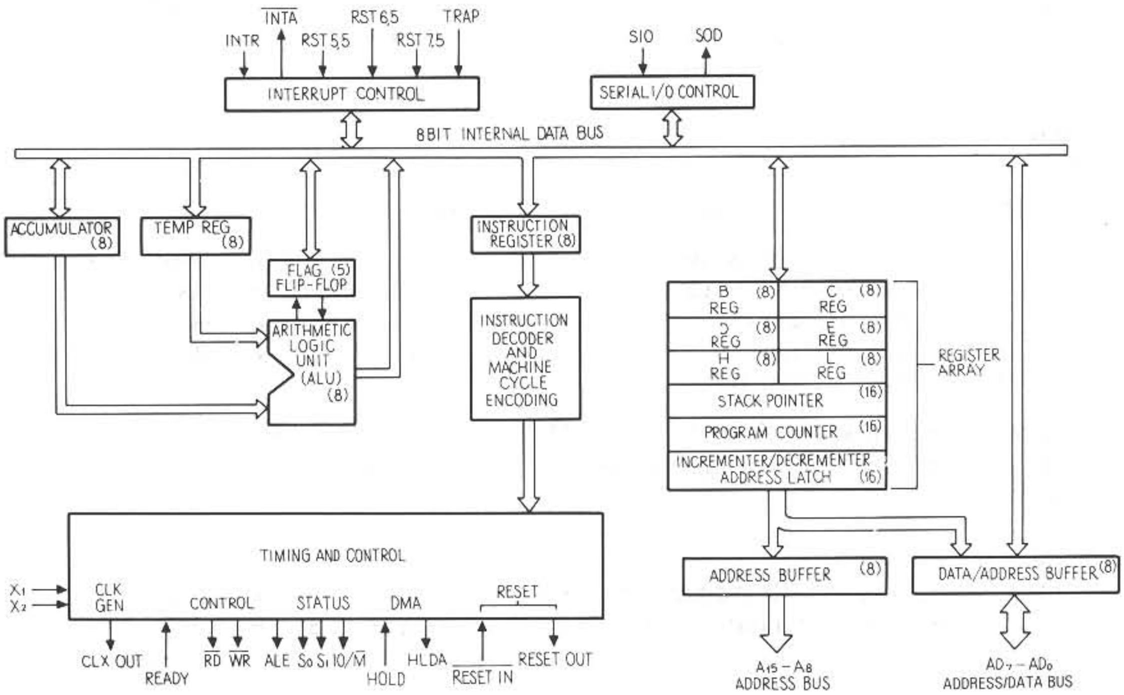


Figure C-1. Functional Block Diagram

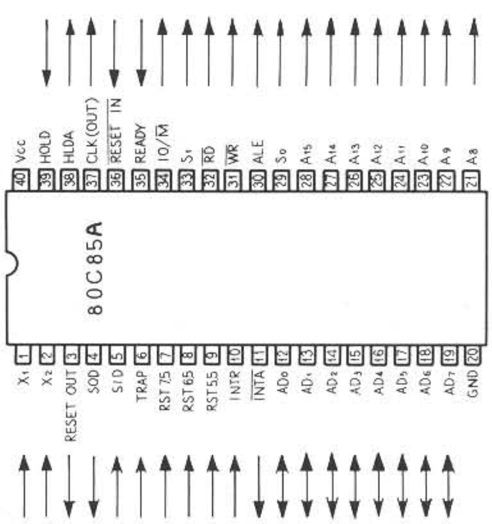


Figure C-2. Pin Configuration of 80C85A

Functional Pin Description

A_8 – A_{15} (Output, 3-state)
Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

AD_0 – AD_7 (Input/Output, 3-state)
Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.

ALE (Output)
Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.

S_0, S_1 and IO/$\overline{M}$
Machine cycle status:

IO/$\overline{M}$	S_1	S_0	States	IO/$\overline{M}$	S_1	S_0	States
0	0	1	Memory write	1	1	1	Interrupt Acknowledge
0	1	0	Memory read	.	0	0	Halt . = 3-state
1	0	1	I/O write	.	×	×	Hold (high impedance)
1	1	0	I/O read	.	×	×	Reset ×= unspecified
0	1	1	Opcode fetch				

S_1 can be used as an advanced R/W status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.

$\overline{RD}$ (Output, 3-state)
READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.

$\overline{WR}$ (Output, 3-state)
WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR, 3-stated during Hold and Halt modes and during RESET.

READY (Input)
If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.

HOLD (Input)
HOLD indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.

HLDA (Output)
HOLD ACKNOWLEDGE: Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.

INTR (Input)
INTERRUPT REQUEST: Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{\text{INTA}}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

$\overline{\text{INTA}}$ (Output)
INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{\text{RD}}$ during the instruction cycle after an INTR is accepted.

RST 5.5, RST 6.5, RST 7.5 (Input)
RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.
The priority of these interrupts is ordered as shown in Table C-1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.

TRAP (Input)
Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same timing as INTR or RST 5.5 – 7.5. It is unaffected by any mask or Interrupt Disable. It has the highest priority of any interrupt. (See Table C-1.)

$\overline{\text{RESET IN}}$ (Input)
Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The CPU is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.

RESET OUT (Output)
Indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.

X_1, X_2 (Input)
X_1 and X_2 are connected to a crystal to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.

CLK (Output)
Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.

SID (Input)
Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (Output)
Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

Vcc
+5 volt supply.

GND
Ground Reference.

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge and high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	(2)	High level until sampled.

Notes: (1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched depends on the instruction provided to the CPU when the interrupt is acknowledged.

Table C-1. Interrupt Priority, Restart Address and Sensitivity

Function

The 80C85A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or a 16-bit register pairs. The 80C85A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8-bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Register; data pointer (HL)	8-bit × 6 or 16-bits × 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flag (8-bit space)

The 80C85A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data Bus. These lower 8-bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 80C85A provides $\overline{RD}$, $\overline{WR}$, S_0, S_1 and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. Hold and all Interrupts are synchronized with the processor's internal clock. The 80C85A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for a simple serial interface.

In addition to these features, 80C85A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

Interrupt and Serial I/O

The 80C85A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table C-1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080A) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{\text{RESET IN}}$ to the 80C85A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP-highest priority, RST 7.5, RST 6.5, RST 5.5, INTR-lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure C-3 illustrates the TRAP interrupt request circuitry within the 80C85A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5 – 7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

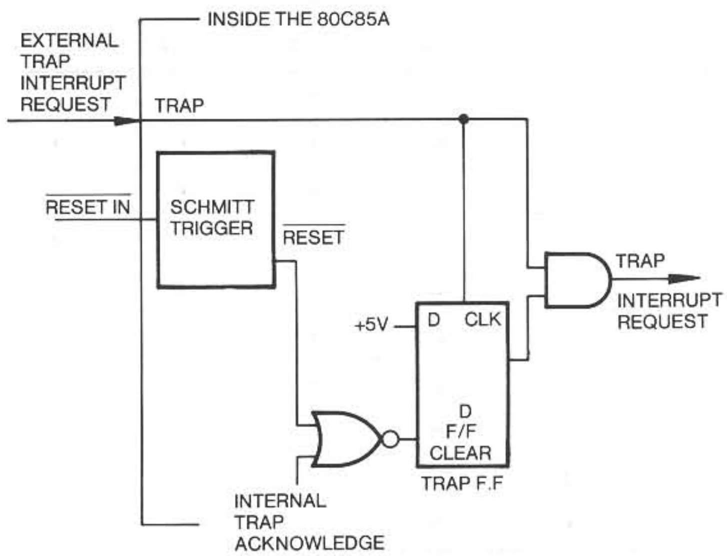


Figure C-3. Trap and $\overline{\text{RESET IN}}$

Basic System Timing

The 80C85A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure C-4 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/$\overline{M}$,S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table C-2.) The status line can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table C-3.

Machine Cycle		Status			Control		
		$IO/\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	(OF)	0	1	1	0	1	1
Memory Read	(MR)	0	1	0	0	1	1
Memory Write	(MW)	0	0	1	1	0	1
I/O Read	(IOR)	1	1	0	0	1	1
I/O Write	(IOW)	1	0	1	1	0	1
Acknowledge of INTR	(INA)	1	1	1	1	1	0
Bus Idle	(BI) : DAD	0	1	0	1	1	1
	ACK. OF						
	RST, TRAP	1	1	1	1	1	1
	HALT	TS	0	0	TS	TS	1

Table C-2. 80C85A Machine Cycle Chart

Machine State	Status & Buses				Control		
	S_1, S_0	$IO/\overline{M}$	$A_8 - A_{15}$	$AD_0 - AD_7$	$\overline{RD}, \overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1 (1)
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0 (2)	X	TS	1	1	0
T_5	1	0 (2)	X	TS	1	1	0
T_6	1	0 (2)	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"
1 = Logic "1"
TS = High Impedance
X = Unspecified

Notes : (1) ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
(2) $IO/\overline{M} = 1$ during $T_4 - T_6$ of INA machine cycle.

Table C-3. 80C85A Machine State Chart

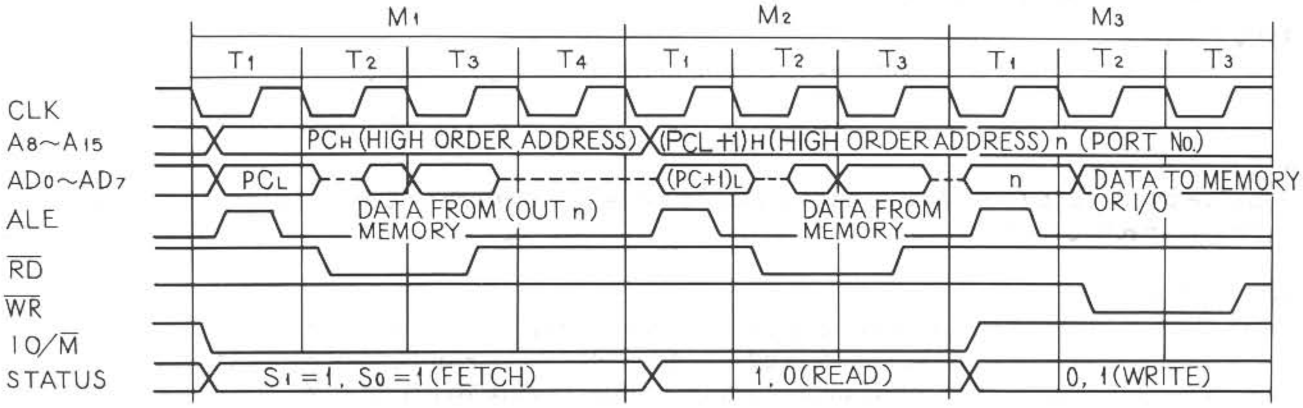


Figure C-4. 80C85A Basic System Timing

C-2. 81C55

General Description

The MSM81C55RS/GS is a 2K bit static RAM (256 byte) with parallel I/O ports. It uses silicon gate CMOS technology and consumes a standby current of 100 micro ampere maximum while the chip is not selected. Featuring a maximum access time of 400 ns, the MSM81C55RS/GS can be used in an 80C85A system without using wait states. The parallel I/O consists of two 8-bit ports and one 6-bit port (both general purpose). The MSM81C55RS/GS also contains a 14-bit programmable counter/timer which may be used for sequence-wave generation or terminal countpulsing.

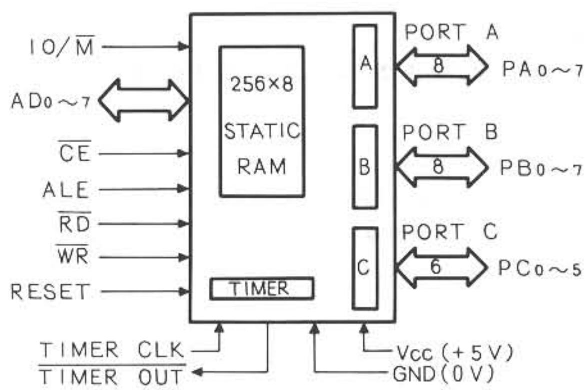


Figure C-5. Functional Block Diagram

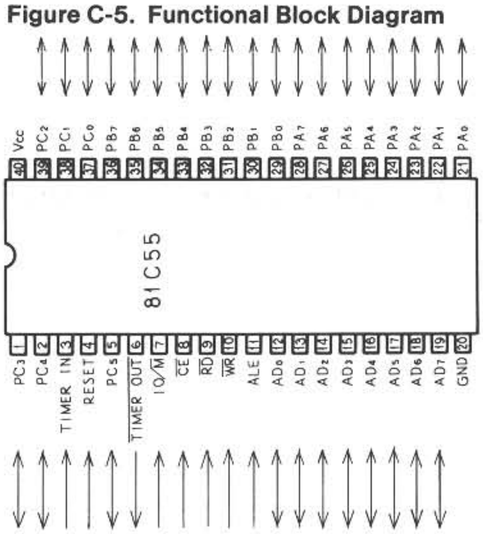


Figure C-6. Pin Configuration of 81C55

Functional Pin Description

RESET (Input)
A high level input to this pin resets the chip, placing all three I/O ports in the input mode, and stops timer.

ALE (Input)
Negative going edge of the ALE (Address Latch Enable) input latches $AD_{0 \sim 7}$, IO/$\overline{\text{M}}$, and CE signals into the respective latches.

$AD_{0 \sim 7}$ (Input/Output)
Three-state, bi-directional address/data bus. Eight-bit address information on this bus is read into the internal address latch at the negative going edge of the ALE. Eight bits of data can be read from or written to the chip using this bus depending on the state of the WRITE or READ input.

$\overline{\text{CE}}$ (Input)
When the CE input is high, both read and write operations to the chip are disabled.

IO/$\overline{\text{M}}$ (Input)
A high level input to this pin selects the internal I/O functions, and a low level selects the memory.

$\overline{\text{RD}}$ (Input)
If this pin is low, data from either the memory or ports is read onto the $AD_{0 \sim 7}$ lines depending on the state of the IO/$\overline{\text{M}}$ line.

$\overline{\text{WR}}$ (Input)
It this pin is low, data on lines $AD_{0 \sim 7}$ is written into either the memory or into the selected port depending on the state of the IO/$\overline{\text{M}}$ line.

$PA_{0 \sim 7}$, $PB_{0 \sim 7}$ (Input/Output)
General-purpose I/O pins. Input/output directions can be determined by programming the command/status (C/S) register.

$PC_{0 \sim 5}$ (Input/Output)
Three pins are usable either as general-purpose I/O pins or control pins for the PA and PB ports. When used as control pins, they are assigned to the following functions:
PC0 : A INTR (port A interrupt)
PC1 : A BF (port A full)
PC2 : A $\overline{\text{STB}}$ (port A strobe)
PC3 : B INTR (port B interrupt)
PC4 : B BF (port B buffer full)
PC5 : B $\overline{\text{STB}}$ (port B strobe)

TIMER IN (Input)
Input to the counter/timer

$\overline{\text{TIMER OUT}}$ (Output)
Timer output. When the present count is reached during timer operation, this pin provides a square-wave or pulse output depending on the programmed control status.

Function

81C55 has 3 functions as described below.

- 2K bit static RAM (256 words × 8 bits)
- Two 8-bit I/O ports (PA and PB) and a 6-bit I/O port (PC)
- 14-bit timer counter

The internal register is shown in the figure below, and the I/O addresses are described in the table below.

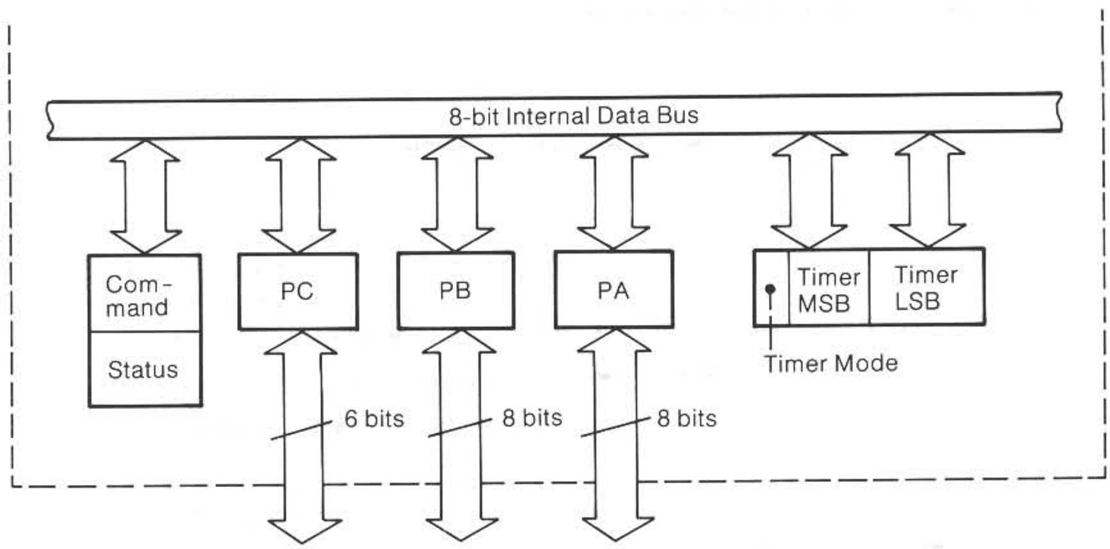


Figure C-7. Internal Register of 81C55

I/O Address								Selecting Register
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Internal command/status register
X	X	X	X	X	0	0	1	Universal I/O port A (PA)
X	X	X	X	X	0	1	0	Universal I/O port B (PB)
X	X	X	X	X	0	1	1	I/O port C (PC)
X	X	X	X	X	1	0	0	Timer count lower position 8 bits (LSB)
X	X	X	X	X	1	0	1	Timer count upper position 6 bits and timer mode 2 bits (MSB)

X : Don't care.

Table C-4. I/O Address of 81C55

(1) Programming the Command/Status (C/S) Register

The contents of the command register can be written during an I/O cycle by addressing it with an I/O address of xxxxx000. Bit assignments for the register are shown below:

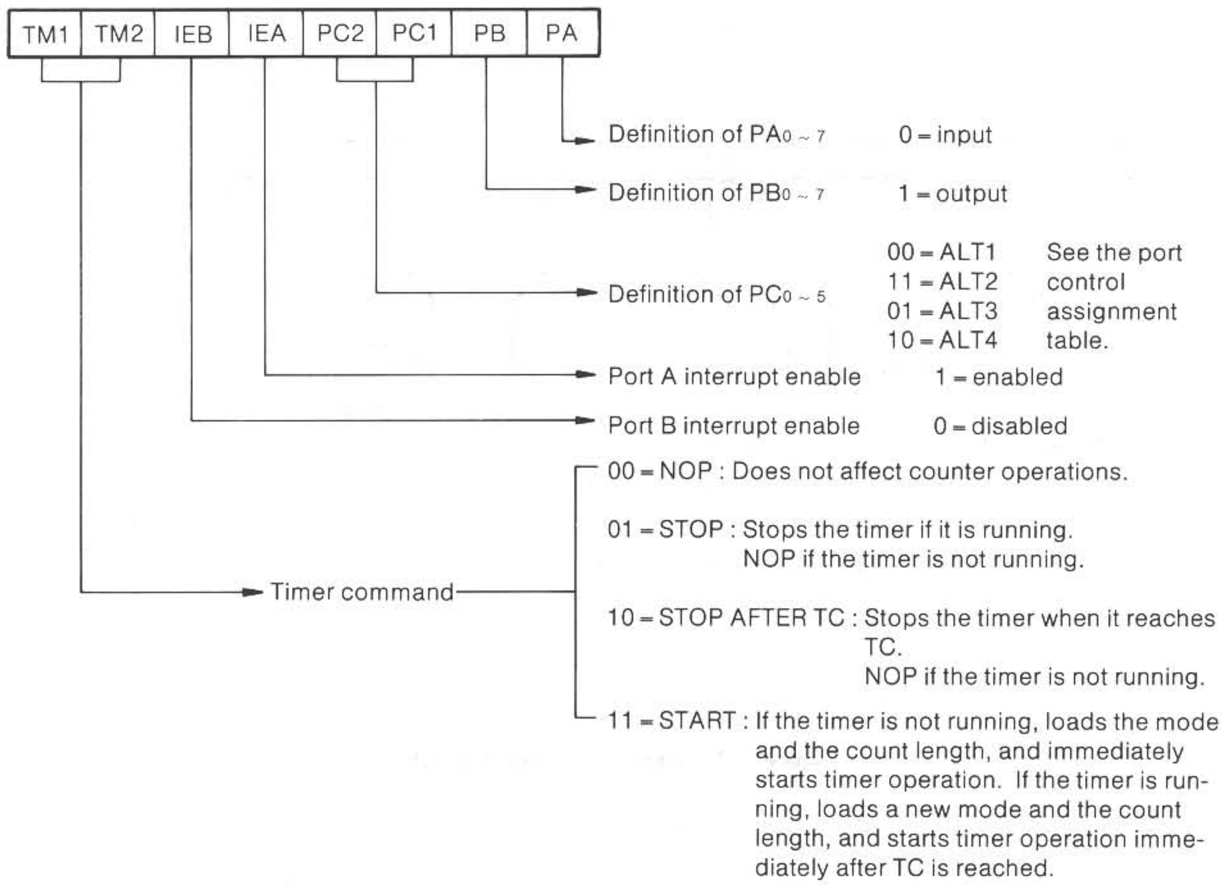


Figure C-8. Programming the Command/Status Register

Pin	ALT1	ALT2	ALT3	ALT4
PC_0	Input port	Output port	A INTR	A INTR
PC_1	Input port	Output port	A BF	A BF
PC_2	Input port	Output port	A STB	A STB
PC_3	Input port	Output port	Output port	B INTR
PC_4	Input port	Output port	Output port	B BF
PC_5	Input port	Output port	Output port	B STB

Table C-5. Port Control Assignment

(2) Reading the C/S Register

The I/O and timer status can be accessed by reading the contents of the Status register located at I/O address xxxxx000. The status word format is shown below:

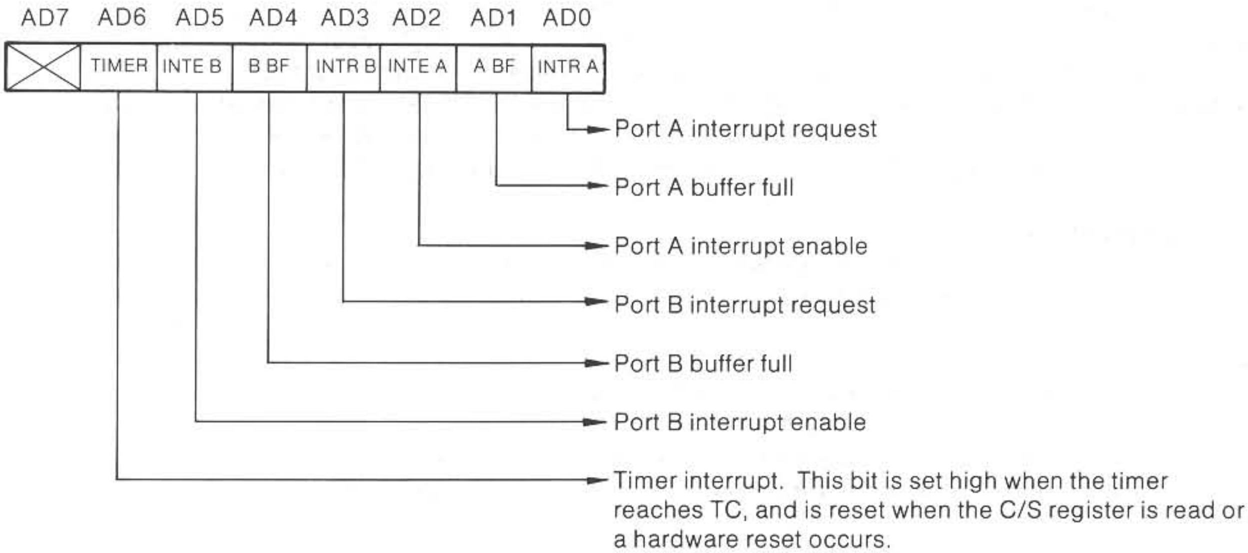


Figure C-9. Reading the C/S Register

(3) PA and PB Registers

These registers may be used as either input or output ports depending on the programmed contents of the C/S register. They may also be used either in the basic mode or in the strobe mode.

I/O address of the PA register : xxxxx001
I/O address of the PB register : xxxxx010

(4) PC Register

The PC register may be used as an input port, output port or control register depending on the programmed contents of the C/S register. The I/O address of the PC register is xxxxx011.

(5) Timer

The timer is a 14-bit counter which counts TIMER IN pulses.

The low order byte of the timer register has an I/O address of xxxxx100, and the high order byte of the register has an I/O address of xxxxx101.

The count length register (CLR) may be preset with two bytes of data. Bits 0 through 13 are assigned to the count length: bits 14 and 15 specify the timer output mode. A read operation of the CLR reads the contents of the counter and the pertinent output mode. The initial value range which can initially be loaded into the counter is 2 through 3FFF hex. Bit assignments to the timer counter and possible output modes are shown in the following.

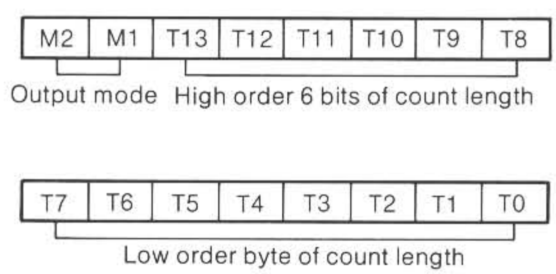


Figure C-10. Bit Assignments to the Timer Counter

M_2	M_1	
0	0	Outputs a low-level signal in the latter half (Note 1) of a count period.
0	1	Outputs a low-level signal in the latter half of a count period, automatically loads the programmed count length, and restarts counting when the TC value is reached.
1	0	Outputs a pulse when the TC value is reached.
1	1	Outputs a pulse each time the preset TC value is reached, automatically loads the programmed count length, and restarts from the beginning.

Note 1 : When counting an asymmetrical value such as (9), a high level is output during the first period of five, and a low level is output during the second period of four.

Note 2 : If an internal counter of the 81C55 receives a reset signal, count operation stops but the counter is not set to a specific initial value or output mode. When restarting count operation after reset, the START command must be executed again through the C/S register.

(6) Standby Mode

The 81C55 is placed in standby mode when the high level at $\overline{CE}$ input is latched during the negative going edge of ALE. All input ports and the timer input should be pulled up or down to either Vcc or GND potential.

When using battery back-up, all ports should be set low or in input port mode. The timer output should be set low. Otherwise, a buffer should be added to the timer output and the battery should be connected to the power supply pins of the buffer.

By setting the reset input to a high level, the standby mode can be selected. In this case, the command register is reset, so the ports automatically set to the input mode and the timer stops.

C-3. 82C51A

General Description

82C51A is USART (Universal Synchronous Asynchronous Receiver Transmitter) for serial data communication developed for the microcomputer system.
As a peripheral device of the microcomputer system, 82C51A receives parallel data from CPU and transmits serial data after conversion. This device also receives serial data from outside and transmits parallel data to CPU after conversion. Thus the device is used for serial data communication.

82C51A configures a fully static circuit using silicon gate CMOS technology. Therefore, it operates on an extremely low power supply at 100 μA (max.) of standby current by suspending all the operations. 82C51A is functionally compatible with 8251A.

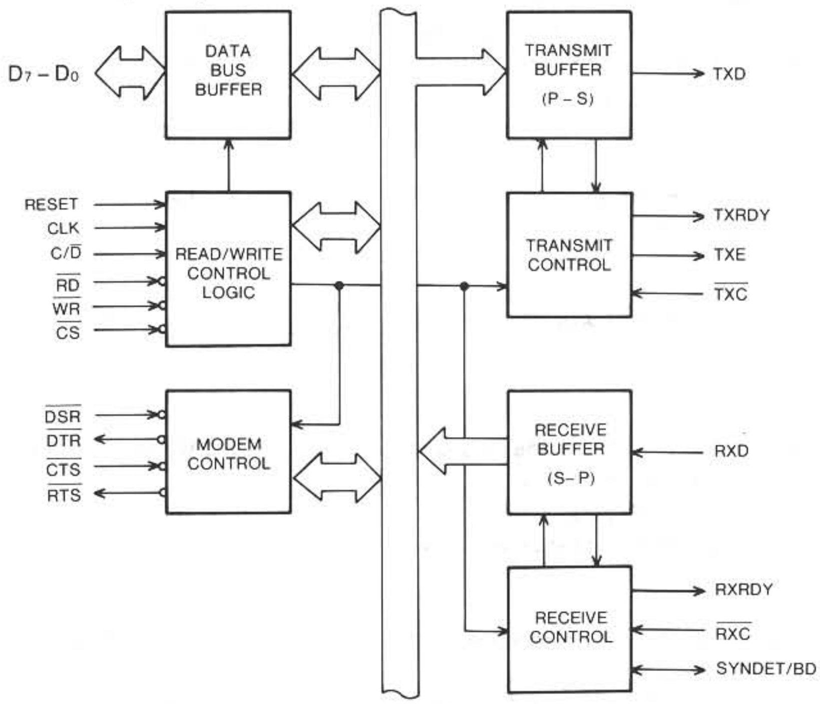


Figure C-11. Functional Block Diagram

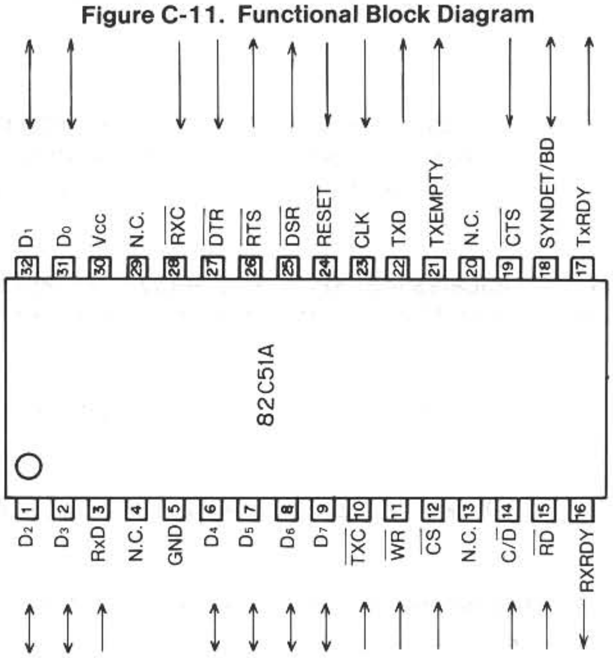


Figure C-12. Pin Configuration of 82C51A

Functional Pin Description

$D_0 - D_7$ (Input/Output)
This is a bidirectional data bus which receives control word and transmit data from CPU and sends status word and received data to CPU.

RESET (Input)
A "High" on this input forces the 82C51A into "reset status".
The device waits for the writing of "mode instruction".
The min. reset width is six clock inputs during the operating status of CLK.

CLK (Input)
CLK signal is used to generate an internal device timing.
CLK signal is independent of $\overline{RXC}$ or $\overline{TXC}$.
However, the frequency of CLK must be greater than 30 times the $\overline{RXC}$ and $\overline{TXC}$ at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

$\overline{WR}$ (Input)
This is "active low" input terminal which receives a signal for waiting transmit data and control words from CPU into 82C51A.

$\overline{RD}$ (Input)
This is "active low" input terminal which receives a signal for reading receive data and status words from 82C51A.

C/$\overline{D}$ (Input)
This is an input terminal which receives a signal for selecting data or command word and status word when 82C51A is accessed by CPU.
If C/$\overline{D}$ = low, data will be accessed.
If C/$\overline{D}$ = high, command word or status word will be accessed.

$\overline{CS}$ (Input)
This is "active low" input terminal which selects the 82C51A at low level when CPU accesses.

> **Note:** The device won't be in "standby status" only setting $\overline{CS}$ = High.
> Refer to "Standby Status".

TXD (Output)
This is an output terminal for transmit data from which serial-converted data is sent out.
The device is in "mark status" (high level) after resetting or during a status when transmit is disable.
It is also possible to set the device in "break status" (low level) by a command.

TXRDY (Output)
This is an output terminal which indicates that 82C51A is ready to accept a transmit data character.
But the terminal is always at low level if $\overline{CTS}$ = high or the device was set in "TX disable status" by a command.

> **Note:** TXRDY of status word indicates that transmit data character is receivable, regardless of $\overline{CTS}$ or command.

If CPU write a data character, TXRDY will be reset by the leading edge or $\overline{WR}$ signal.

TXEMPTY (Output)
This is an output terminal which indicates that 82C51A transmitted all the characters and had no data character.
In "synchronous mode", the terminal is at high level, if transmit data characters are no longer left and sync characters are automatically transmitted.
If CPU write a data character, TXEMPTY will be reset by the leading edge of $\overline{WR}$ signal.

Note: As a transmitter is disabled by setting $\overline{CTS}$ "High"or command, a data written before disabled will be sent out, then TXD and TXEMPTY will be "High". Even if a data is written after disable, that data is not sent out and TXE will be "High".
After enabled transmitter, it is sent out.

$\overline{TXC}$ (Input)
This is a clock input signal which determines the transfer speed of transmit data.
In "synchronous mode", the baud rate will be the same as the frequency of $\overline{TXC}$.
In "asynchronous mode", it is possible to select baud rate factor by mode instruction.
It can be 1, 1/16 or 1/64 the $\overline{TXC}$.
The falling edge of $\overline{TXC}$ shifts the serial data out of the 82C51A.

RXD (Input)
This is a terminal which receives serial data.

RXRDY (Output)
This is a terminal which indicates that 82C51A contains a character that is ready to READ.
If CPU read a data character, RXRDY will be reset by the leading edge of $\overline{RD}$ signal.
Unless CPU reads a data character before next one character is received completely, the preceding data will be lost. In such a case, an overrun error flag of status word will be set.

$\overline{RXC}$ (Input)
This is a clock input signal which determines the transfer speed of receive data.
In "synchronous mode", the baud rate will be the same as the frequency of $\overline{RXC}$.
In "asynchronous mode", it is possible to select baud rate factor by mode instruction.
It can be 1, 1/16, 1/64 the $\overline{RXC}$.

SYNDET/BD (Input/Output)
This is a terminal which function changes according to mode.
In "internal synchronous mode", this terminal is at high level, if sync characters are received and synchronized. If status word is read, the terminal will be reset.
In "external synchronous mode", this is an input terminal.
If "High" on this input forces, 82C51A starts receiving data character.
In "asynchronous mode", this is an output terminal which generates "high level" output upon the detection of "break" character, if receiver data contained "low level" space between stop bits of two continuous characters. The terminal will be reset, if RXD is at high level.

$\overline{DSR}$ (Input)
This is an input port for MODEM interface. The input status of the terminal can be recognized by CPU reading status words.

$\overline{DTR}$ (Output)
This is an output port for MODEM interface. It is possible to set the status of $\overline{DTR}$ by a command.

$\overline{CTS}$ (Input)
This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmit if the device is set in "TX Enable" status by a command.
Data is transmittable if the terminal is at low level.

$\overline{RTS}$ (Output)
This is an output port for MODEM interface. It is possible to set the status of $\overline{RTS}$ by a command.

Function

Outline

82C51A's functional configuration is programed by the software.
Operation between 82C51A and CPU is executed by program control. Table C-6 shows the operation between CPU and the device.

$\overline{CS}$	$C/\overline{D}$	$\overline{RD}$	$\overline{WR}$	
1	X	X	X	Data bus 3-state
0	X	1	1	Data bus 3-state
0	1	0	1	Status → CPU
0	1	1	0	Control word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

Table C-6. Operation between 82C51A and CPU

It is necessary to execute a function-setting sequence after resetting on 82C51A. Figure C-13 shows the function-setting sequence.
If the function was set, the device is ready to receive a command, thus enabling the transfer of data by setting a necessary command, reading a status and reading/writing data.

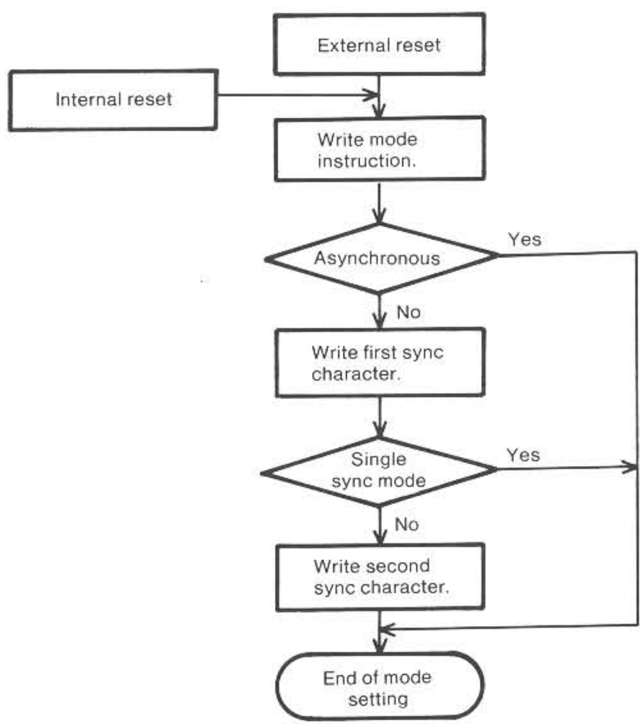


Figure C-13. Function-Setting Sequence (Mode Instruction Sequence)

There are two types of control words.
1. Mode instruction (setting of function)
2. Command (setting of operation)

1. Mode Instruction

Mode instruction is used for setting the function of 82C51A. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of control word after resetting will be recognized as "mode instruction".
Items to be set by mode instruction are as follows:

- Synchronous/Asynchronous mode
- Character hronous mode
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)
- Internal/external synchronization (synchronous mode)
- No. of synchronous characters (synchronous mode)

The bit configuration of mode instruction is shown in Figures C-14 and C-15. In the case of synchronous mode, it is necessary to write one- or two-type sync characters.
If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.

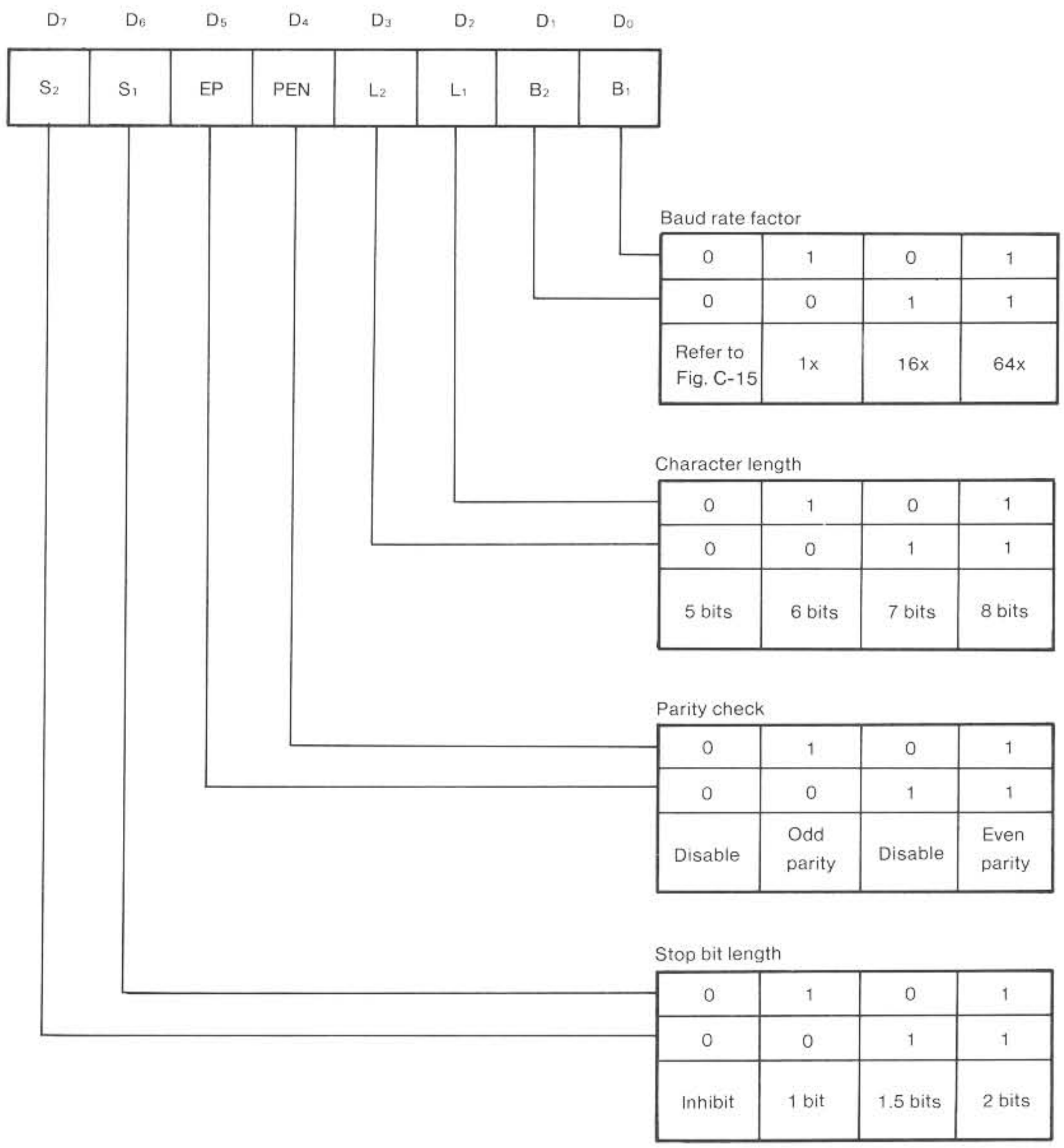


Figure C-14. Bit Configuration of Mode Instruction (Asynchronous)

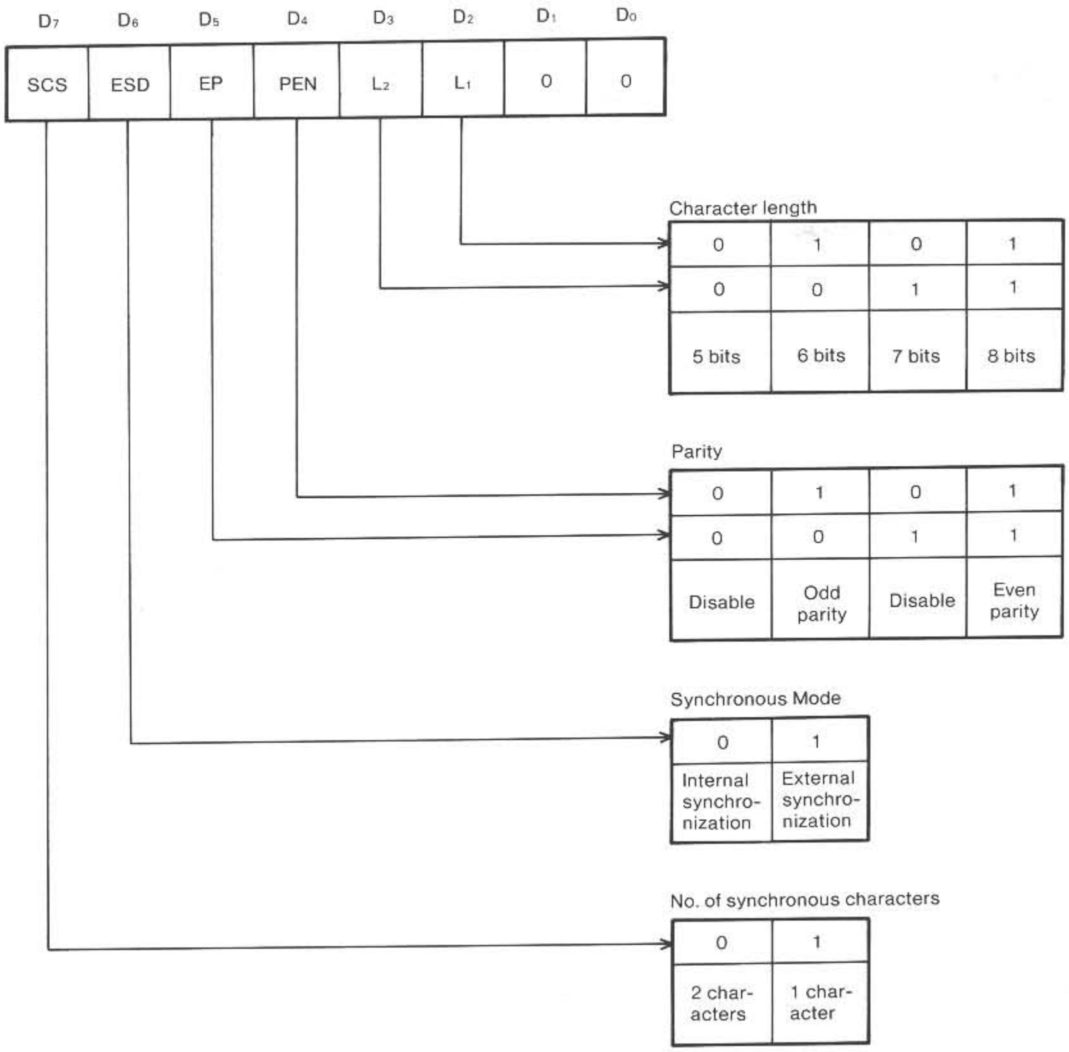


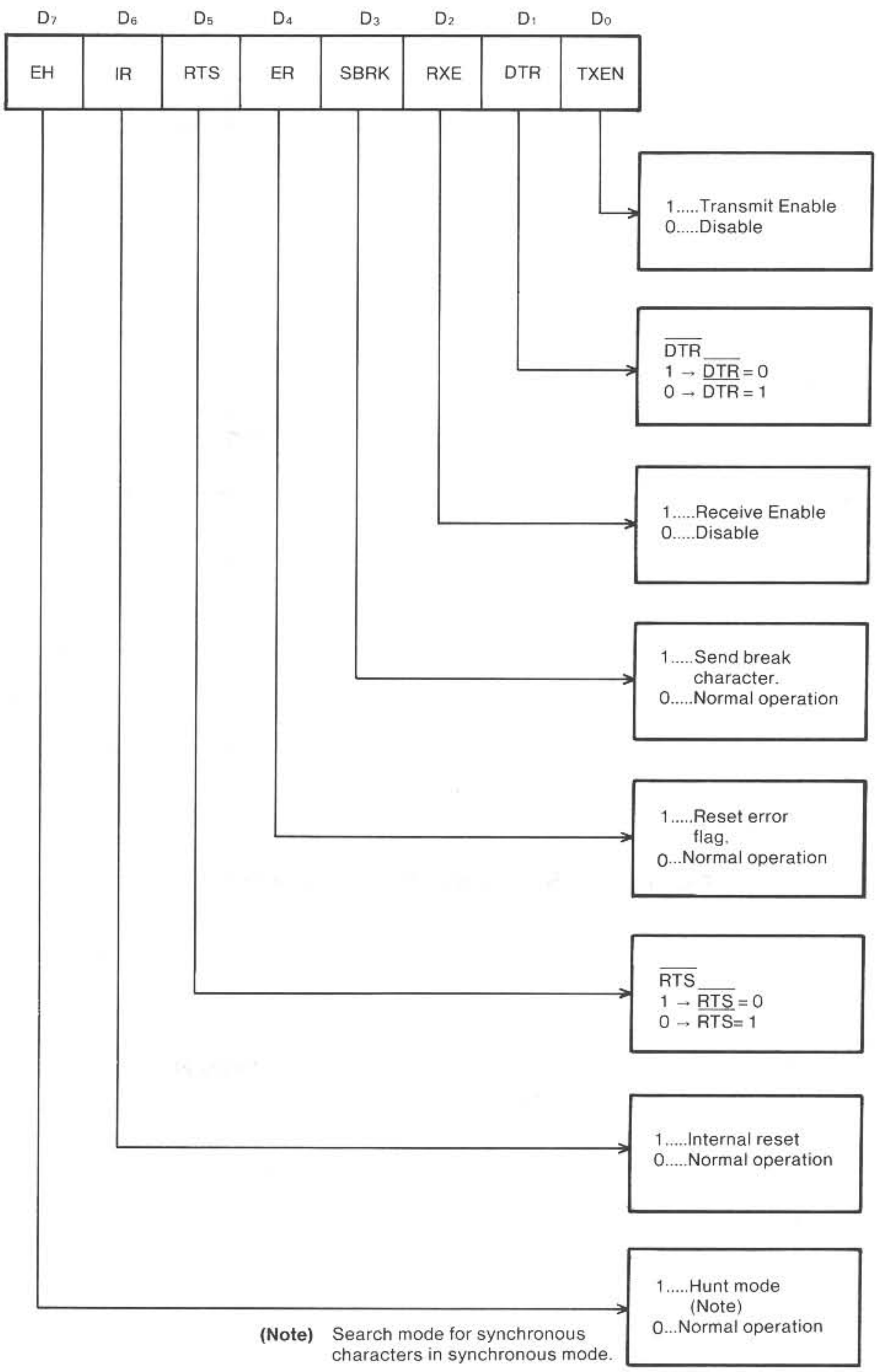
Figure C-15. Bit Configuration of Mode Instruction (Synchronous)

2. Command

Command is used for setting the operation of 82C51A.
It is possible to write a command whenever necessary after writing mode instruction and sync characters.
Items to be set by command are as follows:

- Transmit Enable/Disable
- Receive Enable/Disable
- $\overline{DTR}$, $\overline{RTS}$ Output of data
- Resetting of error flag
- Sending of break characters
- Internal resetting
- Hunt mode (synchronous mode)

The bit configuration of a command is shown in Figure C-16.



(Note) Search mode for synchronous characters in synchronous mode.

Figure C-16. Bit Configuration of Command

Status Word

It is possible to see the internal status of 82C51A by reading a status word. The bit configuration of status word is shown in Figure C-17.

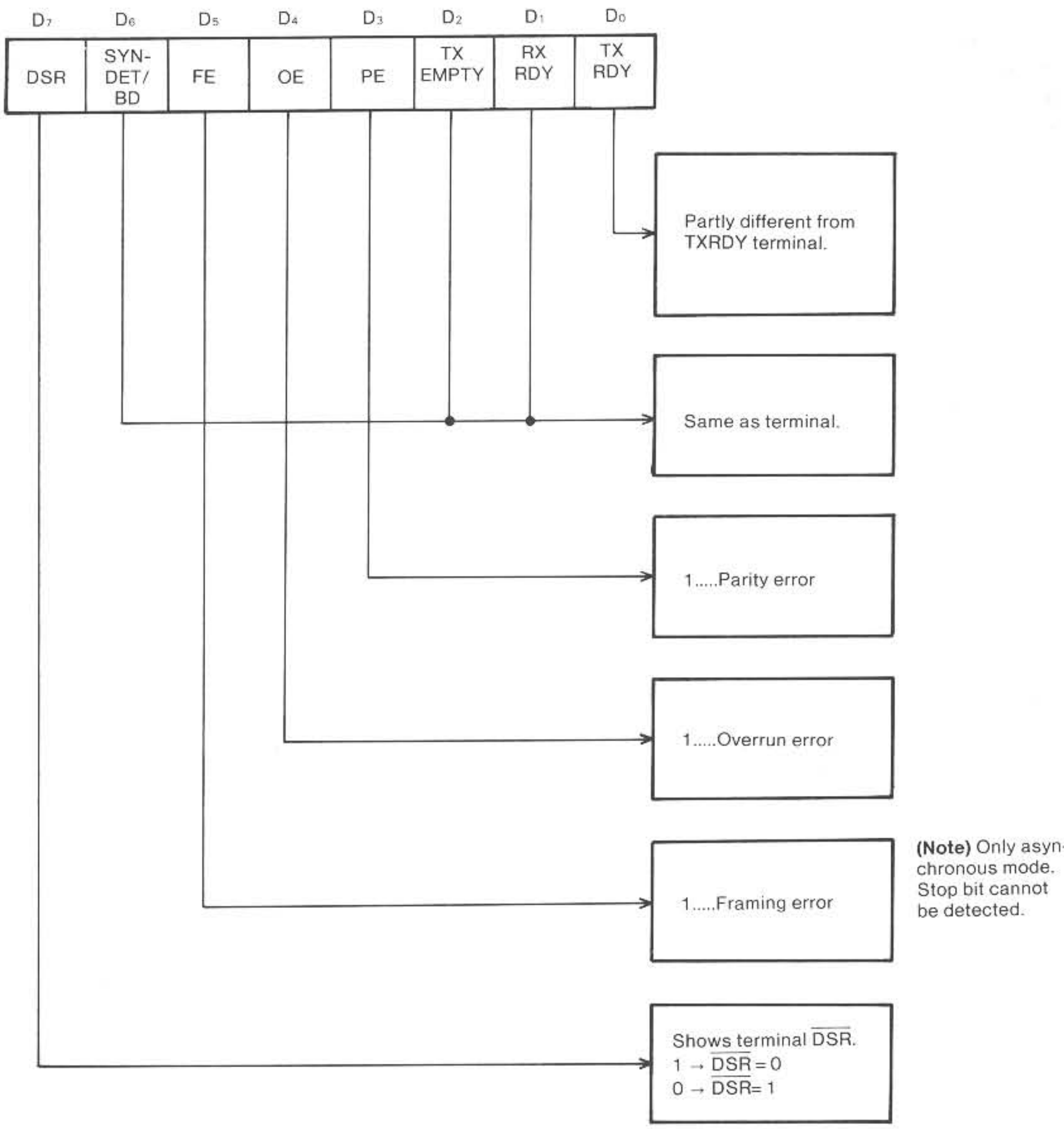


Figure C-17. Bit Configuration of Status Word

Standby Status

It is possible to put 82C51A in "standby status" for the complete static configuration of CMOS. When the following conditions have been satisfied that 82C51A is in "standby status".

- $\overline{CS}$ terminal shall be fixed at VCC level.
- Input pins other than $\overline{CS}$, D0 to D7, $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ shall be fixed at VCC or GND level (including SYNDET in external synchronous mode).

Note: When all outputs current are 0, ICCS specification is applied.

C-4. Basic Construction of LCD

Liquid crystal is a substance midway between a liquid and a solid, although its appearance is much like a liquid. From an electrical and optical stand point, it possesses the properties of a crystal. Items which use this substance are called liquid crystal display elements. The LCD used in the Tandy 200 is a TN (Twisted Nematic) type of liquid crystal. Its basic construction is shown in Figure C-18.

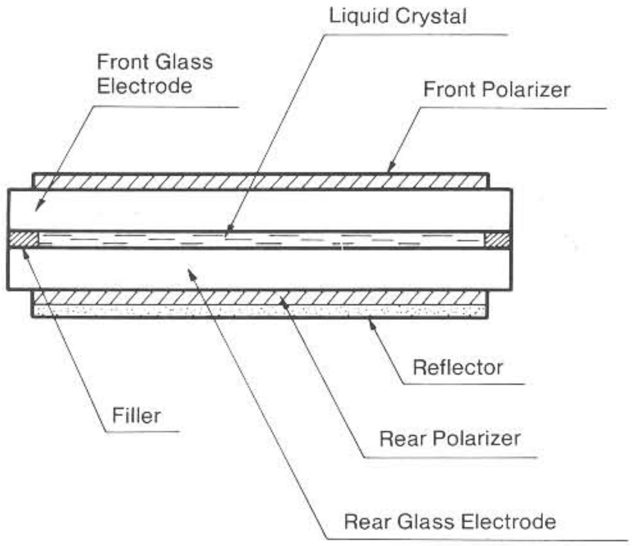


Figure C-18. Construction of LCD Panel

The LCD operates as an "electric shutter" that controls the passage of light.
If voltage is applied, the transmission of light is blocked, otherwise, light is allowed to pass so that letters and numbers can be displayed.

Figure C-19 demonstrates how the LCD operates:

- The liquid-crystal display element is sandwitched between the two polarization plates. The polarized axes of the upper and lower plates are placed at right angles to each other to use the optical "twisting" of light.
- As shown in Figure C-19 (a), if voltage is not applied, the liquid-crystal molecules between the upper and lower plates twist 90° to distribute light. This results in a 90° optical movement and the transmission of light.
- In Figure C-19 (b), however, voltage is applied and the liquid appears frosted in current-carrying areas, thus blocking light transmission.

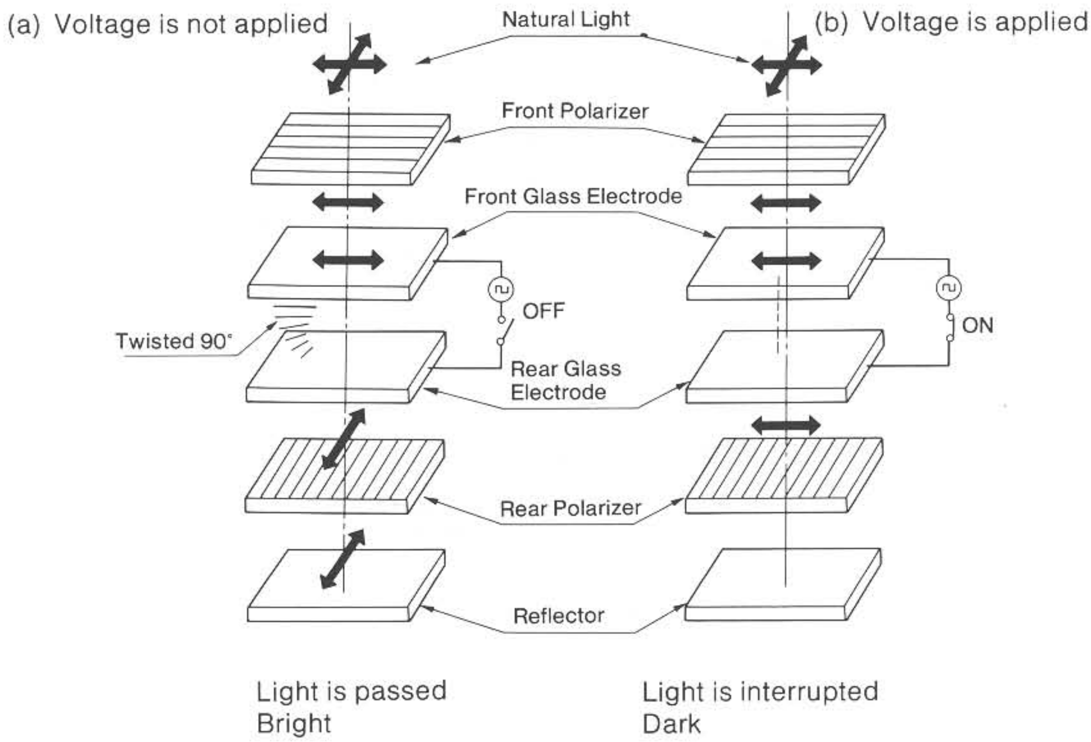


Figure C-19. Operation Theory of LCD Panel

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